Requirements for BeastLink

Xilinx 7 Series FPGAs

BeastLink IP-Core is designed to fit into the trend of IP-based design methodology in Xilinx's Vivado Design Suite. The IP-core is supported only on Xilinx 7-Series FPGAs and Vivado toolchain. It has been tested on the Xilinx Artix-7 FPGA (part xc7a200tfbg676-2).

FX3 Chipset

The BeastLink IP and Software package can be used only with an FX3 chipset. The FX3 Firmware provided with BeastLink configures the FX3 IO pins. In order to use the included FX3 firmware in custom designs, the following pin connections MUST be present.

FX3 Pin	FX3 pin description	FPGA pin	Comments
D4	GPIO[53]	AE16	FPGA_Program_B[1]
D3	GPIO[52]	V11	FPGA_Init_B[1]
D2	GPIO[51]	W10	FPGA_Done.[1]
D1	GPIO[50]	P19	FPGA_CSI_B.[1]
C4	GPIO[57]	-	Power Enable to the FPGA power Supply logic[2]
C1	GPIO[54]	K15	FPGA system Reset.[3] [2] Active HIGH.
F2	GPIO[45]	-	USB_Config_n [4]

NOTE:

The FX3 Firmware configures the FX3 Address, Data and Control pins as per the Cypress-FX3 CYUSB301X datasheet. It is advised not to change the pin configuration.

1 This pin can not be changed in FPGA. FX3 Firmware treats this as a Software settable GPIO.
2 FX3 Firmware treats this as a Software settable GPIO.
3 FPGA pin and FX3 pin can be changed.
4 A logic HIGH level enables FGPA configuration via USB. SPI flash clock MUST be set to tri-state mode prior to enabling USB configuration mode, for example by pulling Program_B low.

Slave FIFO Interface

The FX3 firmware included in BeastLink package configures the FX3 in 16-bit GPIF-II mode during FPGA configuration and in synchronous Slave FIFO interface after configuration. The synchronous Slave FIFO interface uses a 32 bit parallel data bus and several status/control I/O to perform data read/write accesses to EZ-USB FX3's internal FIFO buffers. Register accesses are not done using the Slave FIFO interface. See the following table for a list of connections between FPGA and EZ-USB FX3 used for the host interface.

FX3	FX3 Pin	FPGA Pin	Comment
PCLK	J6	N21, M21	Slave FIFO interface clock[5]; 100MHz
DQ0	F10	T24	Bidirectional data bus bit 0
DQ1	F9	L23	Bidirectional data bus bit 1
DQ2	F7	L22	Bidirectional data bus bit 2
DQ3	G10	L24	Bidirectional data bus bit 3
DQ4	G9	N16	Bidirectional data bus bit 4
DQ5	F8	N17	Bidirectional data bus bit 5
DQ6	H10	R16	Bidirectional data bus bit 6
DQ7	H9	R17	Bidirectional data bus bit 7
DQ8	J10	N18	Bidirectional data bus bit 8
DQ9	J9	K25	Bidirectional data bus bit 9
DQ10	K11	K26	Bidirectional data bus bit 10
DQ11	L10	M20	Bidirectional data bus bit 11
DQ12	K10	L20	Bidirectional data bus bit 12
DQ13	K9	L25	Bidirectional data bus bit 13
DQ14	J8	M24	Bidirectional data bus bit 14
DQ15	G8	M25	Bidirectional data bus bit 15
DQ16	K2	R23	Bidirectional data bus bit 16
DQ17	J4	T23	Bidirectional data bus bit 17
DQ18	K1	R22	Bidirectional data bus bit 18
DQ19	J2	T22	Bidirectional data bus bit 19
DQ20	J3	P26	Bidirectional data bus bit 20

[5] This pin configuration cannot be changed in the FX3. FX3 samples its bidirectional data bus on PCLK. This clock is to be driven by the FPGA. It must be looped back to the FPGA in hardware. The BeastLink IP-core samples the incoming FX3 data on the looped back clock. The input and output clock pins in FPGA can be modified.

FX3	FX3 Pin	FPGA Pin	Comment
DQ21	J1	R26	Bidirectional data bus bit 21
DQ22	H2	T25	Bidirectional data bus bit 22
DQ23	H3	M26	Bidirectional data bus bit 23
DQ24	F4	N26	Bidirectional data bus bit 24
DQ25	G2	P25	Bidirectional data bus bit 25
DQ26	G3	R25	Bidirectional data bus bit 26
DQ27	F3	R21	Bidirectional data bus bit 27
DQ28	F5	R20	Bidirectional data bus bit 28
DQ29	E1	P24	Bidirectional data bus bit 29
DQ30	E5	P23	Bidirectional data bus bit 30
DQ31	E4	N19	Bidirectional data bus bit 31
SLCS#	K8	M22	Chip select for Slave FIFO interface
SLWR#	K7	M19	Write strobe for Slave FIFO interface
SLRD#	H7	K16	Read strobe for Slave FIFO interface
SLOE#	J7	K17	Output enable
PKTEND#	H8	L19	Short packet signal
FLAGA	G7	P21	Flag output from FX3
FLAGB	G6	N24	Flag output from FX3
GPIO23 / CTL[6]	K6	J16	EZ-FX3 GPIO or control output
GPIO25 / CTL[8]	G5	J15	EZ-FX3 GPIO or control output[6]
GPIO26 / CTL[9]	H6	R18	EZ-FX3 GPIO or control output
GPIO27 / CTL[10]	K5	J14	EZ-FX3 GPIO or control output
A0	H5	P20	Address input of Slave FIFO interface
A1	J5	N22	Address input of Slave FIFO interface
GPIO54	C1	K15	FPGA RESET[7]

USB3.0 Port

BeastLink IP-core and Software package give the best performance when deployed in PCs with USB 3.0 ports, preferably in the back-panels. Front-panel USB3.0 ports are not advisable because they are often error-prone. The BeastLink package is backward compatible with USB2.0 too, however, the data rate is lower and when using the system in bus-powered mode, the current supply is much lower than that achievable with USB3.0.

6 Connected to FPGA CCLK during configuration via USB.
7 Software settable active-high reset signal. Used for configuration via USB for synchronization purposes.

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Revision History

Version	Date	Author	Comment
1.0	2018-02-27	VVI	Initial version.

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