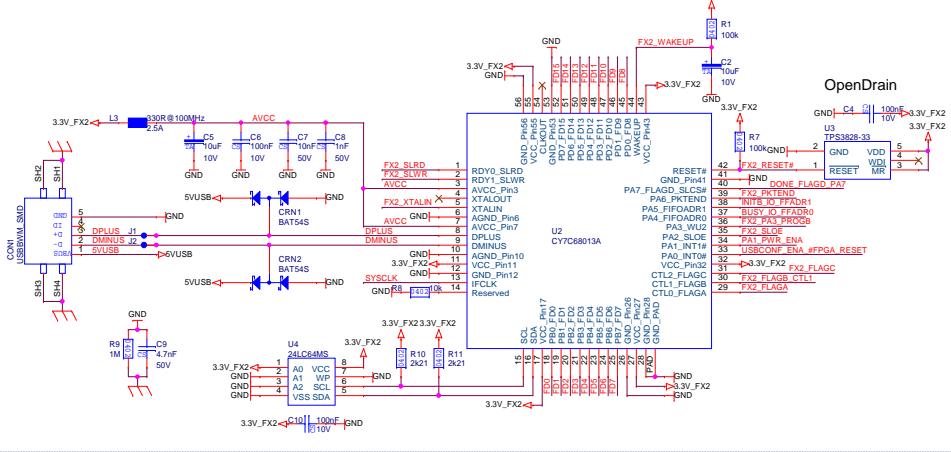


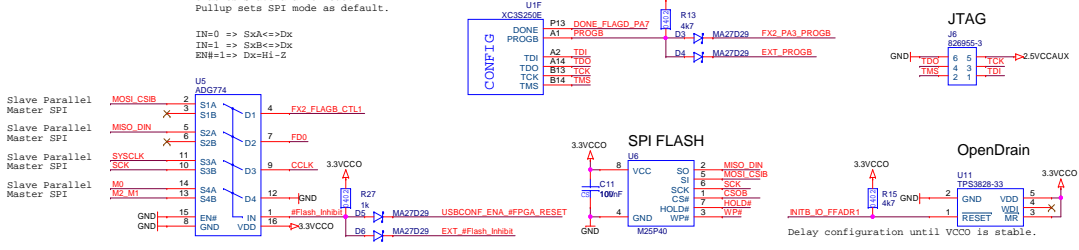
## USB 2.0



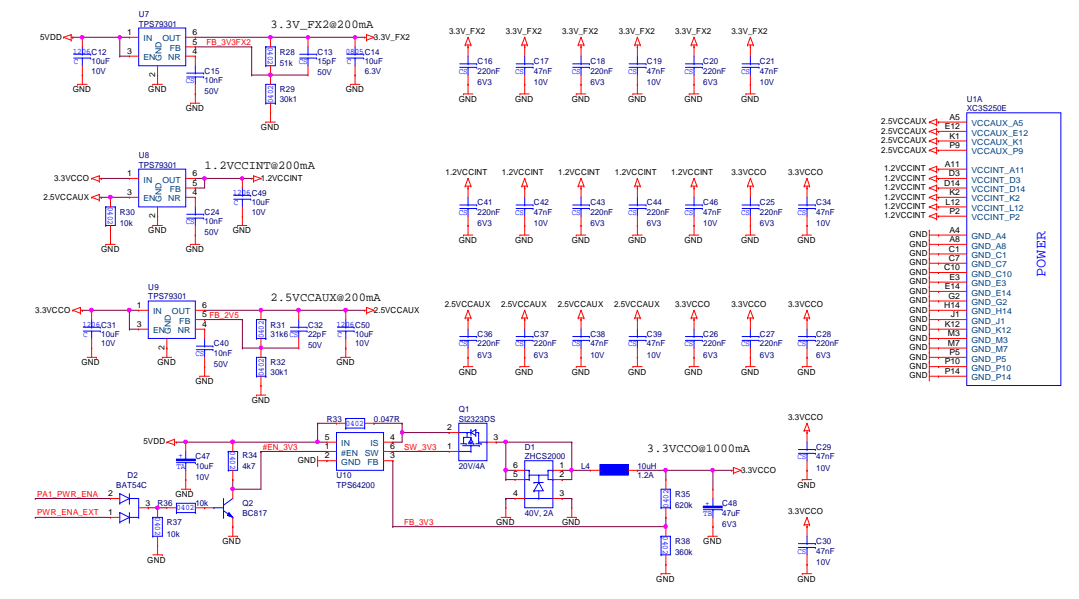
## FPGA I/O



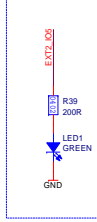
## CONFIGURATION



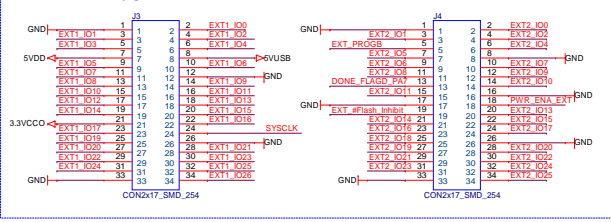
## POWER



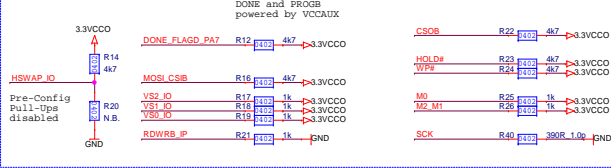
## LED



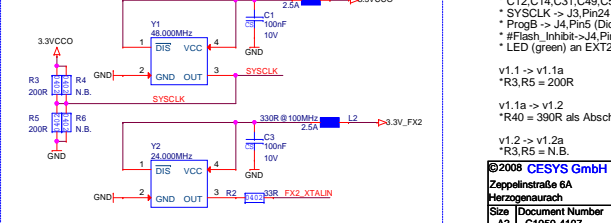
## EXTERNAL I/O



## PULL-UP / -DOWN



## CLOCK



v1.0 -> v1.1  
 \* ResetController for InitB  
 \* C12, C14, C31, C49, C50 durch Keramiktypen ersetzt.  
 \* SYSCLK -> J3, Pin24 => Ext1\_I01B (G12) entfernt  
 \* ProgB -> J4, Pin5 (Diode) => EXT2\_I03 (E2) entfernt  
 \* #Flash\_Inhibit->J4, Pin19(Diode) => EXT2\_I012 (N3) entfernt  
 \* LED (green) an EXT2\_I05

v1.1 -> v1.1a  
 \*R3, R5 = 200R  
 v1.1a -> v1.2  
 \*R40 = 390R als Abschlusswiderstand für SCK eingefügt

v1.2 -> v1.2a  
 \*R3, R5 = N.B.

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