EFM02 – Pinout Expansion Connectors J1 & J2

Revision 1.3 – Last Revised: 14.01.2014

Expansion Connector J1 – ODD

Pin Number	Signal Name	Description	FPGA BUFIO2 Region	FPGA Bank	FPGA IO	XC6SLX150	XC6SLX100	XC6SLX45
1	IO_FPGA_BANK2_OPT_IO22	FPGA I/O.	BL	2	L60N2	R7		
3	IO_FPGA_BANK2_OPT_IO23	FPGA I/O.	BL	2	L60P2	T7		
5	IO_FPGA_BANK2_OPT2_IO9	FPGA I/O. Availability depends on FPGA size.	BL	2	L53P2	Y6	not available	
7	IO_FPGA_BANK2_OPT2_IO8	FPGA I/O. Availability depends on FPGA size.	BL	2	L53N2	W6	not available	
9	IO_FPGA_BANK2_OPT_IO20	FPGA I/O.	BL	2	L47P2	W9		
11	IO_FPGA_BANK2_OPT_IO21	FPGA I/O.	BL	2	L47N2	Y8		
13	1.8V	1.8V Power supply output (VCCO Bank3).						
15	1.8V	1.8V Power supply output (VCCO Bank3).						
17	IO_FPGA_BANK0_OPT_IO9	FPGA I/O. Availability depends on FPGA size.	TL	0	L18N0	H11		not available
19	IO_FPGA_BANK0_OPT_IO8	FPGA I/O. Availability depends on FPGA size.	TL	0	L18P0	G11		not available
21	IO_FPGA_BANK0_IO21	FPGA I/O. Optional GCLK input for Bank 0.	TL	0	L34N0 – GCLK18	A10		
23	IO_FPGA_BANK0_IO20	FPGA I/O. Optional GCLK input for Bank 0.	TL	0	L34P0 – GCLK19	B10		
25	IO_FPGA_BANK0_IO18	FPGA I/O.	TL	0	L33P0	D10		
27	IO_FPGA_BANK0_IO19	FPGA I/O.	TL	0	L33N0	C10		
29	IO_FPGA_BANK0_IO10	FPGA I/O.	TL	0	L6P0	B8		
31	IO_FPGA_BANK0_IO11	FPGA I/O.	TL	0	L6N0	A8		
33	IO_FPGA_BANK0_OPT_IO14	FPGA I/O. Availability depends on FPGA size.	TR	0	L45P0	F13		not available
35	IO_FPGA_BANK0_OPT_IO15	FPGA I/O. Availability depends on FPGA size.	TR	0	L45N0	D13		not available
37	IO_FPGA_BANK0_IO24	FPGA I/O. Optional GCLK input for Bank 0.	TR	0	L36P0 – GCLK15	D11		
39	IO_FPGA_BANK0_IO25	FPGA I/O. Optional GCLK input for Bank 0.	TR	0	L36N0 – GCLK14	C12		
41	IO_FPGA_BANK0_IO29	FPGA I/O.	TR	0	L38N0	A13		
43	IO_FPGA_BANK0_IO28	FPGA I/O.	TR	0	L38P0	C13		
45	IO_FPGA_BANK0_IO33	FPGA I/O.	TR	0	L50N0	A14		
47	IO_FPGA_BANK0_IO32	FPGA I/O.	TR	0	L50P0	B14		
49	IO_FPGA_BANK0_OPT_IO16	FPGA I/O. Availability depends on FPGA size.	TR	0	L46P0	H13		not available
51	IO_FPGA_BANK0_OPT_IO17	FPGA I/O. Availability depends on FPGA size.	TR	0	L46N0	G13		not available
53	IO_FPGA_BANK0_OPT_IO10	FPGA I/O. Availability depends on FPGA size.	TR	0	L43P0	E12		not available
55	IO_FPGA_BANK0_OPT_IO11	FPGA I/O. Availability depends on FPGA size.	TR	0	L43N0	D12		not available
57	IO_FPGA_BANK0_IO30	FPGA I/O.	TR	0	L49P0	D14		
59	IO_FPGA_BANK0_IO31	FPGA I/O.	TR	0	L49N0	C14		
61	IO_FPGA_BANK0_IO35	FPGA I/O.	TR	0	L51N0	A15		
63	IO_FPGA_BANK0_IO34	FPGA I/O.	TR	0	L51P0	C15		
65	IO_FPGA_BANK0_IO22	FPGA I/O. Optional GCLK input for Bank 0.	TL	0	L35P0 – GCLK17	C11		
67	IO_FPGA_BANK0_IO23	FPGA I/O. Optional GCLK input for Bank 0.	TL	0	L35N0 – GCLK16	A11		
69	IO_FPGA_BANK0_OPT_IO20	FPGA I/O. Availability depends on FPGA size.	TR	0	L48P0	F14		not available
71	IO_FPGA_BANK0_OPT_IO21	FPGA I/O. Availability depends on FPGA size.	TR	0	L48N0	H14		not available
73	IO_FPGA_BANK0_IO39	FPGA I/O.	TR	0	L63N0 – SCP6	A16		
75	IO_FPGA_BANK0_IO38	FPGA I/O.	TR	0	L63P0 – SCP7	B16		
77	IO_FPGA_BANK0_IO37	FPGA I/O.	TR	0	L62N0	C16		
79	IO_FPGA_BANK0_IO36	FPGA I/O.	TR	0	L62P0	D15		
81	IO_FPGA_BANK0_IO44	FPGA I/O.	TR	0	L66P0 – SCP1	E16		
83	IO_FPGA_BANK0_IO45	FPGA I/O.	TR	0	L66N0 – SCP0	D17		
85	IO_FPGA_BANK1_IO4	FPGA I/O.	RT	1	L20P1	A20		
87	IO_FPGA_BANK1_IO5	FPGA I/O.	RT	1	L20N1	A21		
89	IO_FPGA_BANK0_IO41	FPGA I/O.	TR	0	L64N0 – SCP4	A17		
91	IO_FPGA_BANK0_IO40	FPGA I/O.	TR	0	L64P0 – SCP5	C17		
93	IO_FPGA_BANK1_OPT_IO0	FPGA I/O.	RT	1	L9P1	G16		
95	IO_FPGA_BANK1_OPT_IO1	FPGA I/O.	RT	1	L9N1	G17		
97	IO_FPGA_BANK1_OPT_IO2	FPGA I/O.	RT	1	L10P1	F16		
99	IO_FPGA_BANK1_OPT_IO3	FPGA I/O.	RT	1	L10N1	F17		
101	IO_FPGA_BANK0_IO43	FPGA I/O.	TR	0	L65N0 – SCP2	A18		
103	IO_FPGA_BANK0_IO42	FPGA I/O.	TR	0	L65P0 – SCP3	B18		
105	IO_FPGA_BANK1_IO2	FPGA I/O.	RT	1	L19P1	B21		
107	IO_FPGA_BANK1_IO3	FPGA I/O.	RT	1	L19N1	B22		
109	IO_FPGA_TDO	FPGA JTAG signal.	NA	NA				
111	IO_FPGA_TMS	FPGA JTAG signal.	NA	NA				
113	IO_FPGA_TCK	FPGA JTAG signal.	NA	NA				
115	IO_FPGA_TDI	FPGA JTAG signal.	NA	NA				
117	IO_FPGA_SUSPEND	FPGA SUSPEND PIN	NA	NA				
119	PWR_ENA_EXT	Drive HIGH to enable FPGA power supplies. (*)						

Expansion Connector J1 – EVEN

Pin Number	Signal Name	Description	FPGA BUFIO2 Region	FPGA Bank	FPGA IO	XC6SLX150	XC6SLX100	XC6SLX45
2	IO_FX3_CLKIN32	FX3 optional 32kHz clock input.						
4	IO_FPGA_Init_B	FPGA INIT_B.						
6	IO_Flash_Inhibit_n	Inhibit FPGA configuration from onboard flash. (**)						
8	IO_FPGA_PROGRAM_B	FPGA Program_B.						
10	IO_FPGA_DONE	FPGA Done.						
12	IO_FPGA_BANK2_OPT_IO26	FPGA I/O.	BL	2	L50P2	U9		
14	IO_FPGA_BANK2_OPT_IO18	FPGA I/O.	BL	2	L46P2	W8		
16	IO_FPGA_BANK2_OPT_IO19	FPGA I/O.	BL	2	L46N2	V7		
18	IO_FPGA_BANK2_OPT2_IO11	FPGA I/O. Availability depends on FPGA size.	BL	2	L54N2	AB5	not available	
20	IO_FPGA_BANK2_OPT2_IO10	FPGA I/O. Availability depends on FPGA size.	BL	2	L54P2	Y5	not available	
22	IO_FPGA_BANK2_OPT_IO7	FPGA I/O.	BL	2	L63N2	V5		
24	IO_FPGA_BANK2_OPT_IO6	FPGA I/O.	BL	2	L63P2	U6		
26	IO_FPGA_BANK2_OPT_IO25	FPGA I/O.	BL	2	L59N2	R8		
28	IO_FPGA_BANK2_OPT_IO24	FPGA I/O.	BL	2	L59P2	R9		
30	IO_FPGA_BANK0_IO8	FPGA I/O.	TL	0	L5P0	C7		
32	IO_FPGA_BANK0_IO9	FPGA I/O.	TL	0	L5N0	A7		
34	IO_FPGA_BANK0_IO14	FPGA I/O.	TL	0	L8P0	C9		
36	IO_FPGA_BANK0_IO15	FPGA I/O.	TL	0	L8N0	A9		
38	IO_FPGA_BANK0_OPT_IO12	FPGA I/O. Availability depends on FPGA size.	TR	0	L44P0	H12		not available
40	IO_FPGA_BANK0_OPT_IO13	FPGA I/O. Availability depends on FPGA size.	TR	0	L44N0	F12		not available
42	IO_FPGA_BANK0_IO4	FPGA I/O.	TL	0	L3P0	D6		
44	IO_FPGA_BANK0_IO5	FPGA I/O.	TL	0	L3N0	C6		
46	IO_FPGA_BANK0_IO16	FPGA I/O.	TL	0	L32P0	D7		
48	IO_FPGA_BANK0_IO17	FPGA I/O.	TL	0	L32N0	D8		
50	IO_FPGA_BANK0_IO13	FPGA I/O.	TL	0	L7N0	C8		
52	IO_FPGA_BANK0_IO12	FPGA I/O.	TL	0	L7P0	D9		
54	IO_FPGA_BANK0_OPT_IO0	FPGA I/O. Availability depends on FPGA size.	TL	0	L14P0	E8		not available
56	IO_FPGA_BANK0_OPT_IO1	FPGA I/O. Availability depends on FPGA size.	TL	0	L14N0	F8		not available
58	IO_FPGA_BANK0_IO3	FPGA I/O.	TL	0	L2N0	A5		
60	IO_FPGA_BANK0_IO2	FPGA I/O.	TL	0	L2P0	C5		
62	IO_FPGA_BANK0_OPT_IO5	FPGA I/O. Availability depends on FPGA size.	TL	0	L16N0	H10		not available
64	IO_FPGA_BANK0_OPT_IO4	FPGA I/O. Availability depends on FPGA size.	TL	0	L16P0	G9		not available
66	IO_FPGA_BANK2_OPT_IO15	FPGA I/O.	BL	2	L40N2	T11		
68	IO_FPGA_BANK2_OPT_IO14	FPGA I/O.	BL	2	L40P2	R11		
70	IO_FPGA_BANK0_OPT_IO2	FPGA I/O. Availability depends on FPGA size.	TL	0	L15P0	G8		not available
72	IO_FPGA_BANK0_OPT_IO3	FPGA I/O. Availability depends on FPGA size.	TL	0	L15N0	F9		not available
74	IO_FPGA_BANK0_IO7	FPGA I/O.	TL	0	L4N0	A6		
76	IO_FPGA_BANK0_IO6	FPGA I/O.	TL	0	L4P0	B6		
78	IO_FPGA_BANK0_OPT_IO6	FPGA I/O. Availability depends on FPGA size.	TL	0	L17P0	E10		not available
80	IO_FPGA_BANK0_OPT_IO7	FPGA I/O. Availability depends on FPGA size.	TL	0	L17N0	F10		not available
82	**VCCO_IO0**	Power supply for FPGA Bank 0. (*** *)		0				
84	**VCCO_IO0**	Power supply for FPGA Bank 0. (*** *)		0				
86	IO_FPGA_BANK0_IO0	FPGA I/O. FPGA HSWAPEN pin. (*** ***)	TL	0	L1P0	A3		
88	IO_FPGA_BANK0_IO1	FPGA I/O.	TL	0	L1N0	A4		
90	IO_FPGA_BANK0_OPT_IO19	FPGA I/O. Availability depends on FPGA size.	TR	0	L47N0	F15		not available
92	IO_FPGA_BANK0_OPT_IO18	FPGA I/O. Availability depends on FPGA size.	TR	0	L47P0	E14		not available
94	IO_FPGA_BANK0_IO26	FPGA I/O. Optional GCLK input for Bank 0.	TR	0	L37P0 – GCLK13	B12		
96	IO_FPGA_BANK0_IO27	FPGA I/O. Optional GCLK input for Bank 0.	TR	0	L37N0 – GCLK12	A12		
98	IO_FPGA_BANK1_OPT_IO6	FPGA I/O.	RT	1	L28P1	H16		
100	IO_FPGA_BANK1_OPT_IO7	FPGA I/O.	RT	1	L28N1	H17		
102	IO_FPGA_BANK1_IO8	FPGA I/O.	RT	1	L30P1	F18		
104	IO_FPGA_BANK1_IO9	FPGA I/O.	RT	1	L30N1	F19		
106	IO_FPGA_BANK1_IO_14	FPGA I/O.	RT	1	L33P1	G19		
108	IO_FPGA_BANK1_IO_15	FPGA I/O.	RT	1	L33N1	F20		
110	IO_FPGA_BANK1_IO0	FPGA I/O.	RT	1	L1P1	C19		
112	IO_FPGA_BANK1_IO1	FPGA I/O.	RT	1	L1N1	B20		
114	**VCCO_3V3**	Power supply output (FPGA Bank 2, VCCAUX and JTAG.)		2				
116	**VCCO_3V3**	Power supply output (FPGA Bank 2, VCCAUX and JTAG.)		2				
118	IO_FPGA_BANK1_IO_12	FPGA I/O.	RT	1	L32P1	C20		
120	IO_FPGA_BANK1_IO_13	FPGA I/O.	RT	1	L32N1	C22		

Expansion Connector J2 – ODD

Pin Number	Signal Name	Description	FPGA BUFIO2 Region	FPGA Bank	FPGA IO	XC6SLX150	XC6SLX100	XC6SLX45
1	**VBUS_IO**	5V power input. (*** **)						
3	**VBUS_IO**	5V power input. (*** **)						
5	**VBUS_CON**	5V power output from onboard USB connector.						
7	IO_SS_TX_M	USB3 TX- Signal.(***)						
9	IO_SS_TX_P	USB3 TX+ Signal.(***)						
11	IO_SS_RX_P	USB3 RX+ Signal.(***)						
13	IO_SS_RX_M	USB3 RX- Signal.(***)						
15	FX3_VIO5	3.3V Power supply output for FX3 I²C interface.						
17	IO_FX3_TCK	FX3 JTAG Interface signal.						
19	IO_FX3_GPIO55	FX3 I/O signal.						
21	IO_FX3_GPIO56	FX3 I/O signal.						
23	not connected							
25	IO_FPGA_BANK2_OPT2_IO6	FPGA I/O. Availability depends on FPGA size.	BL	2	L52P2	T10	not available	
27	IO_FPGA_BANK2_OPT2_IO7	FPGA I/O. Availability depends on FPGA size.	BL	2	L52N2	U10	not available	
29	IO_FPGA_BANK2_OPT2_IO5	FPGA I/O. Availability depends on FPGA size.	BL	2	L51N2	U8	not available	
31	IO_FPGA_BANK2_OPT2_IO4	FPGA I/O. Availability depends on FPGA size.	BL	2	L51P2	T8	not available	
33	IO_FPGA_BANK2_OPT_IO11	FPGA I/O.	BR	2	L20N2	Y14		
35	IO_FPGA_BANK2_OPT_IO10	FPGA I/O.	BR	2	L20P2	W14		
37	IO_FPGA_BANK2_OPT_IO17	FPGA I/O.	BL	2	L44N2	Y10		
39	IO_FPGA_BANK2_OPT_IO16	FPGA I/O.	BL	2	L44P2	W10		
41	IO_FPGA_BANK2_IO0	FPGA I/O. Optional GCLK input for Bank 2.	BL	2	L32P2 – GCLK29	Y11		
43	IO_FPGA_BANK2_IO1	FPGA I/O. Optional GCLK input for Bank 2.	BL	2	L32N2 – GCLK28	AB11		
45	IO_FPGA_BANK2_OPT_IO1	FPGA I/O.	BR	2	L8N2	U16		
47	IO_FPGA_BANK2_OPT_IO0	FPGA I/O.	BR	2	L8P2	U17		
49	IO_FPGA_BANK1_IO63	FPGA I/O.	RB	1	L74N1	T20		
51	IO_FPGA_BANK1_IO62	FPGA I/O. Optional AWAKE output pin.	RB	1	L74P1 – AWAKE	T19		
53	IO_FPGA_BANK1_OPT_IO17	FPGA I/O.	RB	1	L73N1	R19		
55	IO_FPGA_BANK1_OPT_IO16	FPGA I/O.	RB	1	L73P1	P18		
57	IO_FPGA_BANK2_OPT2_IO1	FPGA I/O. Availability depends on FPGA size.	BR	2	L17N2	W15	not available	
59	IO_FPGA_BANK2_OPT2_IO0	FPGA I/O. Availability depends on FPGA size.	BR	2	L17P2	Y16	not available	
61	VCCINT_1V2	1.2V Power supply output (VCCINT).						
63	VCCINT_1V2	1.2V Power supply output (VCCINT).						
65	IO_FPGA_BANK1_IO55	FPGA I/O.	RB	1	L53N1	N19		
67	IO_FPGA_BANK1_IO54	FPGA I/O.	RB	1	L53P1	M19		
69	IO_FPGA_BANK1_IO58	FPGA I/O.	RB	1	L60P1	W20		
71	IO_FPGA_BANK1_IO59	FPGA I/O.	RB	1	L60N1	W22		
73	IO_FPGA_BANK1_OPT_IO11	FPGA I/O.	RB	1	L70N1	V20		
75	IO_FPGA_BANK1_OPT_IO10	FPGA I/O.	RB	1	L70P1	U19		

Expansion Connector J2 – EVEN

Pin Number	Signal Name	Description	FPGA BUFIO2 Region	FPGA Bank	FPGA IO	XC6SLX150	XC6SLX100	XC6SLX45
2	IO_SS_DM	USB2 D- Signal.(***)						
4	IO_SS_DP	USB2 D+ Signal.(***)						
6	IO_OTG_ID	USB OTG ID.(***)						
8	IO_FX3_TRSTn	FX3 JTAG Interface signal.						
10	IO_FX3_TDO	FX3 JTAG Interface signal.						
12	IO_FX3_TMS	FX3 JTAG Interface signal.						
14	IO_FX3_TDI	FX3 JTAG Interface signal.						
16	IO_FX3_RESETn	FX3 Reset input signal.						
18	IO_FX3_SDA	FX3 I²C interface data I/O signal.						
20	IO_FX3_SCL	FX3 I²C interface clock output signal.						
22	not connected							
24	IO_FPGA_RESETn	FPGA reset signal (FX3 GPIO54).		2	L5N2	AB19		
26	IO_FPGA_BANK2_OPT_IO9	FPGA I/O.	BR	2	L18N2	W13		
28	IO_FPGA_BANK2_OPT_IO8	FPGA I/O.	BR	2	L18P2	V13		
30	IO_FPGA_BANK2_OPT2_IO3	FPGA I/O. Availability depends on FPGA size.	BR	2	L22N2	U12	not available	
32	IO_FPGA_BANK2_OPT2_IO2	FPGA I/O. Availability depends on FPGA size.	BR	2	L22P2	T12	not available	
34	IO_FPGA_BANK2_OPT_IO12	FPGA I/O.	BR	2	L23P2	T14		
36	IO_FPGA_BANK2_OPT_IO13	FPGA I/O.	BR	2	L23N2	R13		
38	IO_FPGA_BANK2_OPT_IO3	FPGA I/O.	BR	2	L9N2	V18		
40	IO_FPGA_BANK2_OPT_IO2	FPGA I/O.	BR	2	L9P2	V19		
42	IO_FPGA_BANK1_IO56	FPGA I/O.	RB	1	L59P1	P19		
44	IO_FPGA_BANK1_IO57	FPGA I/O.	RB	1	L59N1	P20		
46	IO_FPGA_BANK1_IO51	FPGA I/O.	RB	1	L51N1	U22		
48	IO_FPGA_BANK1_IO50	FPGA I/O.	RB	1	L51P1	U20		
50	IO_FPGA_BANK1_OPT_IO8	FPGA I/O.	RB	1	L58P1	M16		
52	IO_FPGA_BANK1_OPT_IO9	FPGA I/O.	RB	1	L58N1	L15		
54	IO_FPGA_BANK1_IO17	FPGA I/O.	RT	1	L34N1	H18		
56	IO_FPGA_BANK1_IO16	FPGA I/O.	RT	1	L34P1	H19		
58	IO_FPGA_BANK1_IO21	FPGA I/O.	RT	1	L36N1	K17		
60	IO_FPGA_BANK1_IO20	FPGA I/O.	RT	1	L36P1	J17		
62	IO_FPGA_BANK2_OPT_IO4	FPGA I/O.	BR	2	L10P2	R16		
64	IO_FPGA_BANK2_OPT_IO5	FPGA I/O.	BR	2	L10N2	R15		
66	IO_FPGA_BANK1_OPT_IO14	FPGA I/O.	RB	1	L72P1	P17		
68	IO_FPGA_BANK1_OPT_IO15	FPGA I/O.	RB	1	L72N1	N16		
70	IO_FPGA_BANK1_OPT_IO12	FPGA I/O.	RB	1	L71P1	M17		
72	IO_FPGA_BANK1_OPT_IO13	FPGA I/O.	RB	1	L71N1	M18		
74	IO_FPGA_BANK1_IO61	FPGA I/O.	RB	1	L61N1	K18		
76	IO_FPGA_BANK1_IO60	FPGA I/O.	RB	1	L61P1	L17		

Expansion Connector J2 – ODD

Pin Number	Signal Name	Description	FPGA BUFIO2 Region	FPGA Bank	FPGA IO	XC6SLX150	XC6SLX100	XC6SLX45
77	IO_FPGA_BANK1_IO33	FPGA I/O. Optional GCLK input for Bank 1.	RB	1	L42N1 – GCLK6	L19		
79	IO_FPGA_BANK1_IO32	FPGA I/O. Optional GCLK input for Bank 1.	RB	1	L42P1 – GCLK7	M20		
81	IO_FPGA_USERCLK	Optional clock oscillator.	BR	2	L30N2 – GCLK0 – USERCCLK	AB13		
83	IO_FPGA_VBATT	Decryptor key memory backup power supply input.	NA	NA				(*** *** *)
85	IO_FPGA_SYSCLK	100MHz clock oscillator output (3,3V LVTTL).	BR	2	L29P2 – GCLK3	W12		
87	IO_FPGA_VFS	Decryptor key EFUSE power supply input.	NA	NA				(*** *** *)
89	IO_FPGA_BANK1_IO46	FPGA I/O.	RB	1	L49P1	R20		
91	IO_FPGA_BANK1_IO47	FPGA I/O.	RB	1	L49N1	R22		
93	IO_FPGA_BANK1_IO42	FPGA I/O.	RB	1	L47P1	N20		
95	IO_FPGA_BANK1_IO43	FPGA I/O. Low during configuration.	RB	1	L47N1 – LDC	N22		
97	IO_FPGA_BANK1_IO28	FPGA I/O. Optional GCLK input for Bank 1.	RT	1	L40P1 – GCLK11	K20		
99	IO_FPGA_BANK1_IO29	FPGA I/O. Optional GCLK input for Bank 1.	RT	1	L40N1 – GCLK10	K19		
101	IO_FPGA_BANK1_IO34	FPGA I/O. Optional GCLK input for Bank 1.	RB	1	L43P1 – GCLK 5	J20		
103	IO_FPGA_BANK1_IO35	FPGA I/O. Optional GCLK input for Bank 1.	RB	1	L43N1 – GCLK4	J22		
105	IO_FPGA_BANK1_IO25	FPGA I/O.	RT	1	L38N1	J19		
107	IO_FPGA_BANK1_IO24	FPGA I/O.	RT	1	L38P1	H20		
109	IO_FPGA_BANK1_IO27	FPGA I/O.	RT	1	L39N1	G22		
111	IO_FPGA_BANK1_IO26	FPGA I/O.	RT	1	L39P1	G20		
113	IO_FPGA_BANK1_IO19	FPGA I/O.	RT	1	L35N1	E22		
115	IO_FPGA_BANK1_IO18	FPGA I/O.	RT	1	L35P1	E20		
117	IO_FPGA_BANK1_IO6	FPGA I/O.	RT	1	L29P1	D19		
119	IO_FPGA_BANK1_IO7	FPGA I/O.	RT	1	L29N1	D20		

Expansion Connector J2 – EVEN

Pin Number	Signal Name	Description	FPGA BUFIO2 Region	FPGA Bank	FPGA IO	XC6SLX150	XC6SLX100	XC6SLX45
78	IO_FPGA_BANK1_OPT_IO4	FPGA I/O.	RT	1	L21P1	K16		
80	IO_FPGA_BANK1_OPT_IO5	FPGA I/O.	RT	1	L21N1	J16		
82	IO_FPGA_BANK1_IO52	FPGA I/O.	RB	1	L52P1	V21		
84	IO_FPGA_BANK1_IO53	FPGA I/O.	RB	1	L52N1	V22		
86	IO_FPGA_BANK1_IO48	FPGA I/O.	RB	1	L50P1	T21		
88	IO_FPGA_BANK1_IO49	FPGA I/O.	RB	1	L50N1	T22		
90	IO_FPGA_BANK1_IO44	FPGA I/O. High during configuration.	RB	1	L48P1 – HDC	P21		
92	IO_FPGA_BANK1_IO45	FPGA I/O.	RB	1	L48N1	P22		
94	IO_FPGA_BANK1_IO40	FPGA I/O.	RB	1	L46P1	M21		
96	IO_FPGA_BANK1_IO41	FPGA I/O.	RB	1	L46N1	M22		
98	IO_FPGA_BANK1_IO39	FPGA I/O.	RB	1	L45N1	L22		
100	IO_FPGA_BANK1_IO38	FPGA I/O.	RB	1	L45P1	L20		
102	IO_FPGA_BANK1_IO36	FPGA I/O.	RB	1	L44P1	K21		
104	IO_FPGA_BANK1_IO37	FPGA I/O.	RB	1	L44N1	K22		
106	IO_FPGA_BANK1_IO30	FPGA I/O. Optional GCLK input for Bank 1.	RT	1	L41P1 – GCLK9	H21		
108	IO_FPGA_BANK1_IO31	FPGA I/O. Optional GCLK input for Bank 1.	RT	1	L41N1 – GCLK8	H22		
110	IO_FPGA_BANK1_IO22	FPGA I/O.	RT	1	L37P1	F21		
112	IO_FPGA_BANK1_IO23	FPGA I/O.	RT	1	L37N1	F22		
114	IO_FPGA_BANK1_IO10	FPGA I/O.	RT	1	L31P1	D21		
116	IO_FPGA_BANK1_IO11	FPGA I/O.	RT	1	L31N1	D22		
118	**VCCO_IO1**	Power supply for FPGA Bank 1. (*** *)		1				
120	**VCCO_IO1**	Power supply for FPGA Bank 1. (*** *)		1				

(*)	Normally FX3 controls FPGA power supplies. If FPGA power supplies have to be enabled, regardless of USB connection status drive this pin to a logic HIGH level (LVTTL 3,3V).
(**)	Default FPGA programming at startup is from onboard SPI flash. To prevent SPI configuration, drive this pin to a logic LOW level (LVTTL 3,3V), prior to enabling FPGA power supplies.
(***)	Reserved. Requires special assembly option. See ordering information for more details.
(*** *)	Connected to VCCO_3V3 onboard. Assembly options available to access bank 0 and/or bank 1 VCCO voltages independently to support signal levels other than 3,3V. Requires special assembly option. See ordering information for more details.
(*** **)	Board is powered via 5V power input. Either connect VBUS_CON output or an adequate 5V power supply.
(*** ***)	4,7kOhm resistor pull-up to VCCO_IO0 connected onboard.
(*** *** *)	XC6SLX45 does not support AES encryption.

FPGA BUFIO2 Region Description

TL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 0 (top).
TR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 0 (top).
RT	I/O clock is driven by any one of the four BUFIO2s located in the top side of bank 1 (right).
RB	I/O clock is driven by any one of the four BUFIO2s located in the bottom side of bank 1 (right).
BL	I/O clock is driven by any one of the four BUFIO2s located in the left side of bank 2 (bottom).
BR	I/O clock is driven by any one of the four BUFIO2s located in the right side of bank 2 (bottom).

		XC6SLX45	XC6SLX100	XC6SLX150
Total available FPGA–IO	Single- Ended	169	179	191
	Differential	84	89	95
Total shared FPGA-IO	Single- Ended	157		
	Differential	78		

Revision history

26.08.13	Preliminary release	
13.11.13	v1.1	Updates due to hardware changes in revision 1.1: * J1,odd: Pins 1, 3, 5, 7, 9, 11, 13, 15 * J1,even: Pins 12, 14, 16, 18, 20, 22, 24 * J2, odd: Pins 19, 23, 61, 63 * J2, even: Pins 22, 24
07.01.14	v1.2	Completed BUFIO2 region information
14.01.14	v1.3	Corrected pin-out: * J1,Pin5; J1,Pin7 * J2,Pin37; J2,Pin39