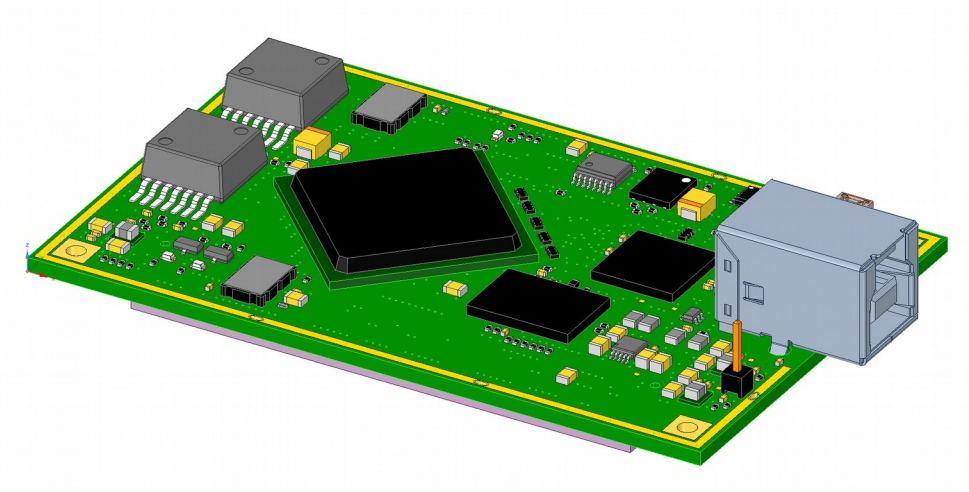
EFM-02B / EFM-02[1]
Hardware reference

(Hardware Revision: Rev.A / 1.3[1])

The EFM-02B- is an embedded module featuring a XILINX™ SPARTAN-6 FPGA in conjunction with the CYPRESS™ FX3 SuperSpeed USB 3.0 interface controller.



Target applications

- Image processing
- Video capture
- Smart cameras
- High-speed FPGA co-processor
- Custom test equipment

1 EFM-02 with USB micro-B connector (obsolete)

Features

- USB3.0 SuperSpeed interface through versatile Cypress™ EZ-FX3 controller
- USB bus-powered, no external power supply necessary
- Optional self-powered mode available
- 32bit Slave FIFO interface
- Two FX3 GPIO on expansion connector
- Xilinx™ Spartan-6 FPGA (LX45, LX100 or LX150)
- Up to 191 single-ended (95 differential) IOs on high-quality high-speed Samtec™ connectors (QSE-060-01), including several GCLK inputs
- 157 single-ended (78 differential) IOs identical throughout EFM-02B line-up
- Independent power supply option for FPGA bank 0 and/or bank 1
- 2Gbit DDR2 memory
- 64Mbit dual SPI configuration/data memory
- High stability 100MHz +/-25ppm onboard clock oscillator
- Mounting position for optional user clock oscillator (industry standard 5mm*7mm)
- 1Mbit (512kbit[1]) I²C EEPROM for FX3 configuration data
- I²C interface available on expansion connector to increase available FX3 configuration memory for standalone applications
- FPGA configuration from SPI memory, JTAG or USB
- One user, two status leds
- JTAG for FPGA and FX3 controller available on expansion connectors
- Small sized PCB only measures 52,6mm x 82,6mm

EFM-02B block diagram

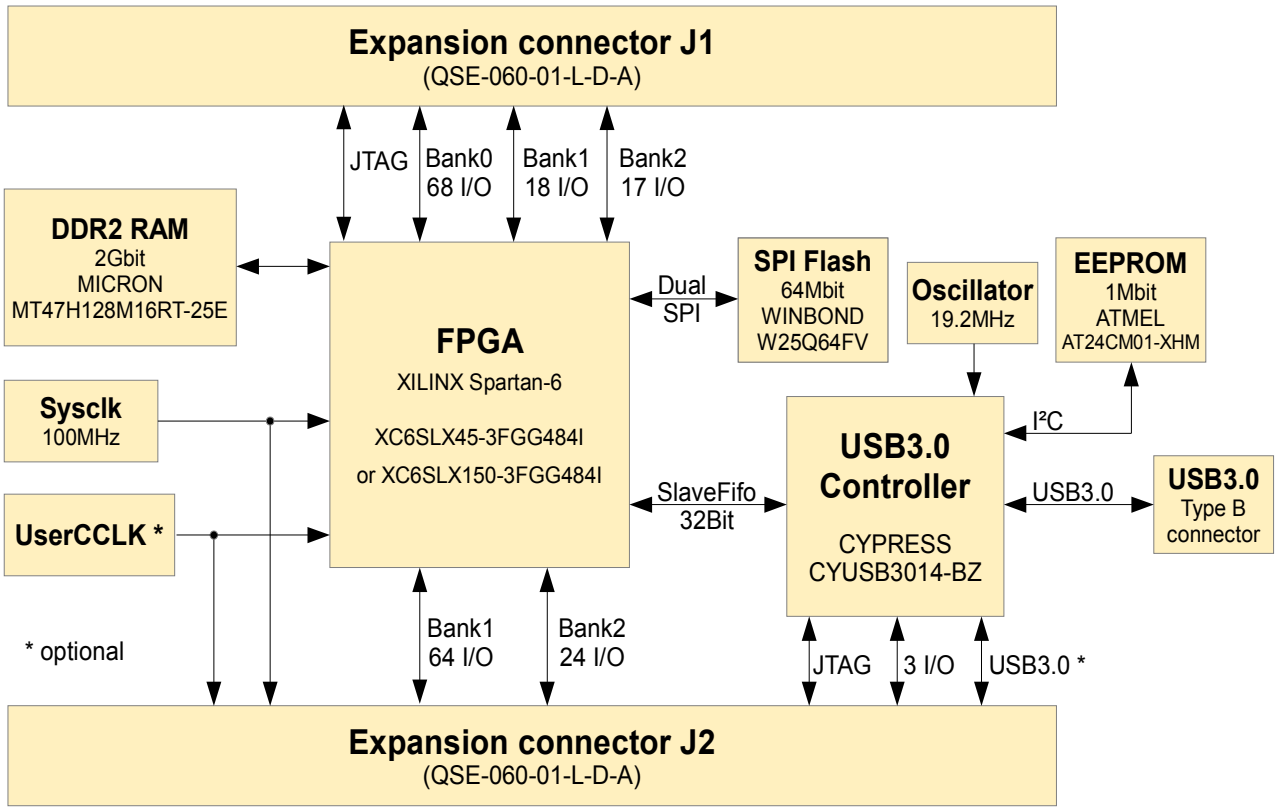


Figure 1: EFM-02B functional block diagram

Specification

Mechanical drawings of the EFM-02B module are shown at the end of this document. The small sized PCB only measures 52,6mm x 82,6mm. Four electrically isolated mounting holes of size M2-fine are located in the corners of the PCB. The fifth mounting hole, located next to the USB3.0 type B connector, provides access to the USB shielding. The two 120-pin expansion connectors J1 and J2 are located on the bottom

side. In addition to up to 191 FPGA I/O- and three FX3 GPIO- signals, JTAG- signals for FPGA and FX3, as well as power supplies are accessible at J1 and J2. Special assembly options of the EFM-02B modules also provide the possibility to independently access VCCO supply voltages of FPGA bank 0 and bank 1 and/or access to USB signals. Please see the ordering information for more details.

Parameter	Min.	Typ.	Max.	Units
Dimensions (B x W)		52,6 x 82,6		mm
Maximum part height on top side besides USB Type B connector		4,8		mm
Maximum part height on bottom side		2,5		mm
Module stacking height[2]	5,0		25,0	mm
Operating temperature range	0°C		60°C	°C

FPGA density

EFM-02B is offered with various assembly options. Off-the-shelf EFM-02B is available with two different Spartan-6 FPGAs. See the following table for more details on the differences between the FPGAs. For more detailed information please consult Xilinx™ documentation. Please also see ordering information for more details on available options.

Feature	XC6SLX45	XC6SLX150
Logic Cells	43 661	147 443
Slices	6 822	23 038
Flip-Flops	54 576	184 304
Distributed RAM (Kbit)	401	1 355
DSP48A1 slices	58	180
Block RAM (Kbit)	2 088	4 824
Clock Management Tiles	4	6
Bitstream length (bit)	11 939 296	33 909 664
Expansion I/Os	169 (84 DIFF)	191 (95 DIFF)

2 Depends on mating QTE connector height.

FPGA Configuration

The FPGA on EFM-02B modules can be loaded with a valid configuration file in one of several ways.

SPI Flash

The on-board serial flash device Winbond W25Q64FV is the default source for configuration bitstreams at startup. Depending on the length of the bitstream which varies with the Spartan-6 FPGA density and design, two or more configuration files can be stored inside the 64Mbit flash device and MultiBoot is supported. To store an appropriate configuration file in flash, several ways exist.

Loading SPI Flash via USB

The easiest way to write configuration data into the on-board SPI flash is to use CESYS **UDK3 Board Manager**. It uses the USB 3.0 interface of the board to write raw binary FPGA configuration bitstreams (*.bin) into the on-board SPI flash. The UDK3 Board Manager is explained in CESYS user guide UG103.

Indirect Programming using FPGA JTAG chain

Another way to configure the SPI flash is by using the Xilinx™ Platform Cable (not included in the EFM-02B scope of delivery) and the Xilinx™ iMPACT programming software. iMPACT requires *.mcs PROM files. In indirect mode iMPACT downloads a small FPGA helper design that provides connection from the iMPACT software through the Spartan-6 device to the SPI flash. Select W25Q64 SPI Flash PROM Type when asked. To speed up FPGA configuration from serial flash, user designs can increase configuration clock frequency or use SPI Dual-Read mode. For more information, read Xilinx™ application note XAPP586 and Xilinx™ Spartan-6 configuration user guide UG380 .

Prevent SPI configuration at startup

Default configuration at startup is from the serial SPI flash device. To prevent starting from SPI flash, set Flash_Inhibit_n to a logic low level prior to enabling FPGA power

supplies. After configuration using a different programming interface, Flash_Inhibit_n has to be released before access to the SPI flash is possible again.

Pin-number	Signal name	Comment
J1, pin 6	Flash_Inhibit_n	Active-low input to prevent programming of FPGA from SPI flash device at startup.

USB

EFM-02B also supports direct reprogramming of the Spartan-6 FPGA via USB without altering the SPI flash content. USB configuration is available at all times, as long as FPGA power supplies are enabled. Use CESYS **UDK3 Board Manager** or the suitable function call from the CESYS UDK API to download the *.bin configuration file. Configuring the FPGA over USB 3.0 is much faster than all other options.

JTAG

The FPGA JTAG interface is routed to the expansion connector J1. All necessary pull-up resistors are already installed on the EFM-02B module. Configuration through the JTAG interface is available at all times, as long as FPGA power supplies are enabled. The JTAG programming voltage is fixed to the 3,3V VCCAUX power supply voltage, which is available at connector J1 as well.

JTAG signal name	J1 pin-number	FPGA direction	Comment
TDO	109	Out	Test data out
TMS	111	In	Test mode select
TCK	113	In	Test clock
TDI	115	In	Test data in
VCCAUX	114,116	--	3,3V JTAG programming voltage

Power supply options

The EFM-02B can be operated from a single 5.0V power source supplied at pins 1 and 3 of the expansion connector J2. On-board high-efficiency switching regulators provide all necessary power supplies: 3,3V, 1,8V, 1,2V. A low-dropout regulator is used to derive the 0,9V DDR2 termination voltage from 1,8V. The 5,0V USB3.0 VBUS power supply is available at pin 5 of the expansion connector J2, the 3,3V power supply is connected to pins 114 and 116 of J1. The EFM-02B is designed to support both USB power supply schemes: bus-powered and self-powered mode.

Bus-powered mode

In bus-powered mode pins 1 and 3 of the expansion connector J2 **MUST** be connected to the 5,0V USB3.0 VBUS power supply, which is provided at pin 5 of J2. Either install jumper J4 or plug EFM-02B module into an adequate board. Please be sure to remove jumper J4 in case an external power supply should be used. Otherwise EFM-02B or connected devices may be damaged.
According to the USB specifications, the FPGA power supplies are only switched on, when an USB connection has been established and FX-3 firmware has been downloaded successfully. PWR_ENA_EXT on pin 119 of J1 MUST be left open for bus-powered mode to work properly.

Self-powered mode

In self-powered mode, connect an adequate external 5,0V power supply to J2 pins 1 and 3. Pin 5 of J2, which connects to USB3.0 VBUS power supply, should be left open. Please make sure that jumper J4 is not installed. Otherwise EFM-02B or attached devices may be damaged. NEVER connect an external power supply to J2, pin 5, as this may damage the host computers USB peripheral interface. Similar to bus-powered mode, internal logic controls the generation of FPGA power supplies and only activates these, when an USB connection has been established and FX-3 firmware has been downloaded successfully. If FPGA power supplies shall be enabled regardless of the USB connection state, PWR_ENA_EXT on pin 119 of J1 must be driven to a logic HIGH level or connected to the external 5,0V power supply. Then all necessary on-board power supplies are enabled as soon as the external 5,0V power supply becomes available.

Power supply mode		J2, Pins 1,3	J2, Pin 5	J1, Pin 119
Bus-powered		Either install jumper J4 or plug EFM-02B into an adequate breakout board which connects these pins.		open
Self-powered	USB controlled	Connect to external 5,0V power supply.	open	open
	Instant on	Connect to external 5,0V power supply.	open	Connect to external 5.0V power supply or drive to a logic HIGH level.

External power supply input requirements	Min.	Typ.	Max.	Units
Power supply input range at J2, Pins 1+3	4,5	5	5,5	V
Minimum current requirement	250			mA

On-board peripherals

With plenty of FPGA I/O available at the expansion connectors the EFM-02B supports a vast number of applications. To help the system designer to successfully implement a Spartan-6 design some crucial peripherals are installed on-board, with a VHDL reference design EFM02_soc readily available.

Dual SPI configuration/data memory

The on-board serial flash device Winbond W25Q64FV provides 64Mbit of non-volatile storage. The flash is connected to the configuration interface of the FPGA and serves as default configuration medium. Depending on bitstream length, two or more FPGA configuration files can be stored in flash allowing MultiBoot operation. Remaining free storage can be used in user designs. The W25Q64FV supports standard Serial Peripheral Interface as well as the faster Dual SPI. SPI clock frequencies of up to 104MHz are supported allowing data rates beyond 25MByte/s in Dual SPI mode.

SPI Flash	FPGA Pin	FPGA Direction	Comment
DI (MISO0)	AB20	Output (Input)	Serial data output (input)
DO (MISO1)	AA20	Input	Serial data input
CLK	Y21[3]	Output	Serial clock
#CS	T5	Output	Chip select
#WP	--	--	Write protect[4]
#HOLD	--	--	Hold[4]

3 Connected only when FPGA configuration via USB is disabled (default mode).
4 Pull-up resistor connected onboard EFM-02B.

DDR2 memory

The EFM-02B module provides 2Gbit of high-speed DDR2 memory connected to FPGA bank 3, which is supplied by an on-board 1,8V switching power supply. The following table shows detailed information about the connections.

DDR2	FPGA Pin	FPGA Direction	Comment
DQ0	N3	Bidirectional	Bidirectional data bus bit 0
DQ1	N1	Bidirectional	Bidirectional data bus bit 1
DQ2	M2	Bidirectional	Bidirectional data bus bit 2
DQ3	M1	Bidirectional	Bidirectional data bus bit 3
DQ4	J3	Bidirectional	Bidirectional data bus bit 4
DQ5	J1	Bidirectional	Bidirectional data bus bit 5
DQ6	K2	Bidirectional	Bidirectional data bus bit 6
DQ7	K1	Bidirectional	Bidirectional data bus bit 7
LDM	L4	Output	Data mask for lower byte
LDQS	L3	Bidirectional	Data strobe for lower byte
#LDQS	L1	Bidirectional	Data strobe for lower byte
DQ8	P2	Bidirectional	Bidirectional data bus bit 8
DQ9	P1	Bidirectional	Bidirectional data bus bit 9
DQ10	R3	Bidirectional	Bidirectional data bus bit 10
DQ11	R1	Bidirectional	Bidirectional data bus bit 11
DQ12	U3	Bidirectional	Bidirectional data bus bit 12
DQ13	U1	Bidirectional	Bidirectional data bus bit 13
DQ14	V2	Bidirectional	Bidirectional data bus bit 14
DQ15	V1	Bidirectional	Bidirectional data bus bit 15
UDM	M3	Output	Data mask for upper byte
UDQS	T2	Bidirectional	Data strobe for upper byte
#UDQS	T1	Bidirectional	Data strobe for upper byte
A0	H2	Output	Address input bit 0
A1	H1	Output	Address input bit 1
A2	H5	Output	Address input bit 2
A3	K6	Output	Address input bit 3
A4	F3	Output	Address input bit 4
A5	K3	Output	Address input bit 5
A6	J4	Output	Address input bit 6
A7	H6	Output	Address input bit 7
A8	E3	Output	Address input bit 8
A9	E1	Output	Address input bit 9
A10	G4	Output	Address input bit 10

DDR2	FPGA Pin	FPGA Direction	Comment
A11	C1	Output	Address input bit 11
A12	D1	Output	Address input bit 12
A13	G6	Output	Address input bit 13
BA0	G3	Output	Bank address input
BA1	G1	Output	Bank address input
BA2	F1	Output	Bank address input
#RAS	K5	Output	Command input
#CAS	K4	Output	Command input
#WE	F2	Output	Command input
ODT	J6	Output	On-die termination
CK	H4	Output	Differential memory clock
#CK	H3	Output	Differential memory clock
CKE	D2	Output	Clock enable
#CS	--	--	Chip select[5]
--	Y2	--	100 ohms resistor for MIG on-chip termination
--	W3	--	Not connected pin for MIG

The Spartan-6 FPGA provides hardware memory control blocks for communication with DDR2 memory devices. The component MT47H128M16RT-25E from Micron™ is suitable for DDR2-800 timings at a #CAS latency of five and is fully supported by the Xilinx™ memory interface generator (MIG). You are strongly encouraged to read and understand the Micron™ data sheet as well as Xilinx™ documentation on MIG and the Spartan-6 memory controller blocks.

Maximum DDR2 memory clock frequency with Spartan-6 devices not only depends on the FPGA speedgrade, but also on VCCINT power supply. The EFM-02B has a high-efficiency switching regulator with very low output voltage ripple to generate an adequate VCCINT power supply necessary for the so-called "Extended Performance Mode". In conjunction with the -3 speedgrade of the Spartan-6 devices used on the EFM-02B as default assembly option DDR2 clock frequencies up to 800MHz are possible.

Mode	Speedgrade	Maximum DDR2 clock frequency
Normal	-2	625MHz
Normal	-3	667MHz
Extended	-2	667MHz
Extended	-3	800MHz

5 Externally pulled LOW.

Status leds

Two leds give basic information about power and configuration status of the EFM-02B module.

Led	Function	Comment
LED1	DONE	Lights up, when FPGA is configured correctly.
LED3	POWER	Lights up, when FPGA power supply is enabled.

LED1 connects to the FPGA DONE output signal. Whenever a valid configuration file is stored within FPGA SRAM, LED1 will light up. LED3 is connected to the FPGA power supplies such that it turns on as soon as the FPGA power supply is enabled, either USB controlled or externally activated through PWR_ENA_EXT on pin 119 of J1.

User led

LED2 is controllable through FPGA pin A2. Use it for additional user specific status information. A HIGH level output will turn the led on.

Led	FPGA Pin	Comment
LED2	A2	Set HIGH to light up led.

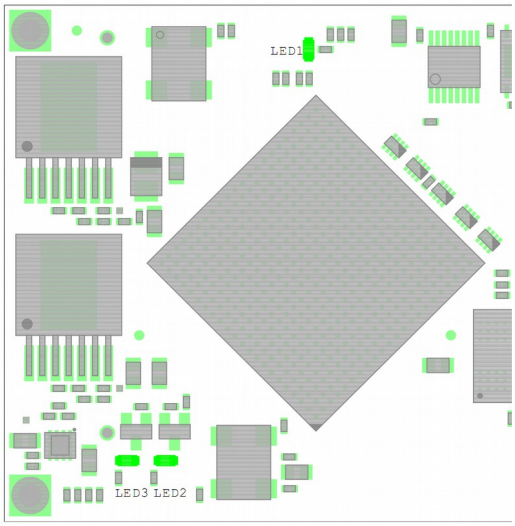


Figure 2: LEDs on top side

On-board clocks

EFM-02B offers two mounting positions for industry standard 5mm * 7mm, 4 pad crystal oscillators. Both clock networks are connected to bank 2 of the Spartan-6 device, which is powered by an on-board 3,3V switching regulator.

High-stability system clock oscillator

With the FXO- series oscillator EFM-02B provides an extremely low jitter 100MHz system clock, available at FPGA ball W12. FPGA internal PLL / DCM can be used to generate a multitude of clock signals. The system clock network also is connected to the expansion connector J2 at pin 85. See the following table for some specifications.

Parameter	Value
Frequency	100MHz
Frequency stability	+/-25ppm[6]
Maximum output low voltage	0,33V
Minimum output high voltage	2,97V
Maximum output load	30pF
Cycle rise/fall time	3ns

Optional clock oscillator

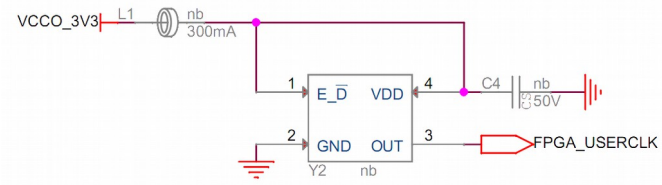


Figure 4: Schematic diagram for optional user clock oscillator Y2.

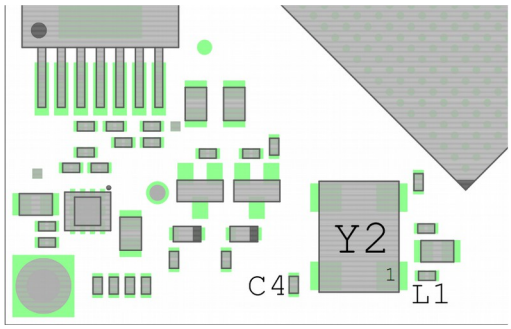


Figure 3: Mounting position for optional clock oscillator Y2.

For applications requiring clock signals not producible from the 100MHz system clock EFM-02B provides a mounting position for a second user definable clock oscillator. Footprint and pin-out comply to industry standard 5mm * 7mm, 4 pad layouts.

6 Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

The optional user clock network is connected to FPGA ball AB13 and to the expansion connector J2 at pin 81. For designs demanding predictable boot times, it can be used as external clock source for the Master SPI configuration from the on-board SPI flash W25Q64FV, instead of the rather imprecise FPGA internal CCLK oscillator. Please see Xilinx™ Spartan-6 configuration user guide for more details on USERCCLK.

SuperSpeed USB3.0

EFM-02B provides a SuperSpeed USB3.0[7] interface using the versatile controller CYUSB3014-BZ from Cypress Semiconductor. To keep up with the enormously high USB 3.0 data rates, a 32bit Slave FIFO interface running at 100 MHz is used for communication between FPGA and the EZ-USB FX3. See CESYS UG104 for benchmarks and CESYS UG100 for a close description of a slave-fifo interface reference design.

I²C EEPROM

EFM-02B includes the 1Mbit Atmel™ AT24CM01-XHM I²C EEPROM to store VID/PID data for the USB enumeration process.

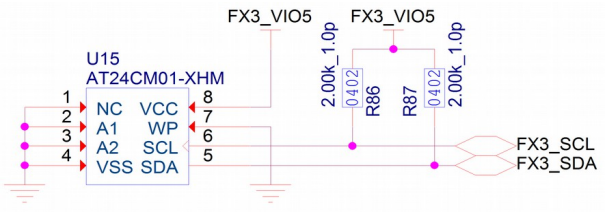


Figure 5: EZ-USB FX3 I²C EEPROM

In case you decide to develop your own FX3 firmware and store it inside non-volatile memory rather than downloading it via USB, it may be required to increase the available memory due to the size of FX3 firmware images. To increase available storage EZ-USB FX3 supports multiple EEPROM devices of the same size and type sharing the I²C bus. The firmware image then should be stored across the EEPROMs as a contiguous image as in a single I²C device. On more information about EZ-FX3 boot options using the I²C interface please consult the application note AN76405 from Cypress™. EZ-USB FX3's I²C interface is available at the expansion connector J2.

FX3	Exp.	FX3 Direction	Comment
FX3_SDA	J2, 18	Bidirectional (Open drain)	I²C interface data line
FX3_SCL	J2, 20	Output (Open drain)	I²C interface clock signal
VIO5	J2, 15		I²C power supply output
GND	J2, GND		GND power terminal

7 Please note, that EZ-USB FX3 boot loader works in USB2.0 mode. With EFM-02 / EFM-02B the default boot mode is via USB, therefore USB2.0 D+/D- lines are still required, even if user applications would only use SuperSpeed USB3.0 mode.

Slave FIFO interface

The synchronous Slave FIFO interface uses a 32bit parallel data bus and several status/control I/O to perform data read/write accesses to EZ-USB FX3's internal FIFO buffers. Register accesses are not done using the Slave FIFO interface. See the following table for a list of connections between FPGA and EZ-USB FX3 used for the host interface.

FX3	FPGA Pin	FPGA Direction	Comment
PCLK	W11/Y12	Output/Input	Slave FIFO interface clock
DQ0	AB21(AA20[8])	Bidirectional	Bidirectional data bus bit 0
DQ1	U14	Bidirectional	Bidirectional data bus bit 1
DQ2	U13	Bidirectional	Bidirectional data bus bit 2
DQ3	AA6	Bidirectional	Bidirectional data bus bit 3
DQ4	AB6	Bidirectional	Bidirectional data bus bit 4
DQ5	W4	Bidirectional	Bidirectional data bus bit 5
DQ6	Y4	Bidirectional	Bidirectional data bus bit 6
DQ7	Y7	Bidirectional	Bidirectional data bus bit 7
DQ8	AA2	Bidirectional	Bidirectional data bus bit 8
DQ9	AB2	Bidirectional	Bidirectional data bus bit 9
DQ10	V15	Bidirectional	Bidirectional data bus bit 10
DQ11	AA18	Bidirectional	Bidirectional data bus bit 11
DQ12	AB18	Bidirectional	Bidirectional data bus bit 12
DQ13	Y13	Bidirectional	Bidirectional data bus bit 13
DQ14	AA12	Bidirectional	Bidirectional data bus bit 14
DQ15	AB12	Bidirectional	Bidirectional data bus bit 15
DQ16	AB15	Bidirectional	Bidirectional data bus bit 16
DQ17	V9	Bidirectional	Bidirectional data bus bit 17
DQ18	AB16	Bidirectional	Bidirectional data bus bit 18
DQ19	AA16	Bidirectional	Bidirectional data bus bit 19
DQ20	T15	Bidirectional	Bidirectional data bus bit 20
DQ21	AB17	Bidirectional	Bidirectional data bus bit 21
DQ22	T16	Bidirectional	Bidirectional data bus bit 22
DQ23	AB10	Bidirectional	Bidirectional data bus bit 23
DQ24	V17	Bidirectional	Bidirectional data bus bit 24
DQ25	AB14	Bidirectional	Bidirectional data bus bit 25
DQ26	Y15	Bidirectional	Bidirectional data bus bit 26
DQ27	Y18	Bidirectional	Bidirectional data bus bit 27
DQ28	W17	Bidirectional	Bidirectional data bus bit 28

8 Connected only when FPGA configuration via USB is enabled.

FX3	FPGA Pin	FPGA Direction	Comment
DQ29	W18	Bidirectional	Bidirectional data bus bit 29
DQ30	T17	Bidirectional	Bidirectional data bus bit 30
DQ31	T18	Bidirectional	Bidirectional data bus bit 31
#SLCS	AB3	Output	Chip select for Slave FIFO interface
#SLWR	AB4	Output	Write strobe for Slave FIFO interface
#SLRD	AB9	Output	Read strobe for Slave FIFO interface
#SLOE	Y3	Output	Output enable
PKTEND	AB8	Output	Short packet signal
FLAGA	AA8	Input	Flag output from FX3
FLAGB	AA14	Input	Flag output from FX3
GPIO23 / CTL[6]	Y17	Input	EZ-FX3 GPIO or control output
GPIO25 / CTL[8]	AA21(Y21[8])	Input	EZ-FX3 GPIO or control output (FPGA CCLK[8])
GPIO26 / CTL[9]	V11	Input	EZ-FX3 GPIO or control output
GPIO27 / CTL[10]	AA10	Input	EZ-FX3 GPIO or control output
CTL[15]	AA4	Input	EZ-FX3 control output (16Bit modes only)
A0	Y19	Output	Address input of Slave FIFO interface
A1	Y9	Output	Address input of Slave FIFO interface
GPIO54	AB19	Input	FPGA_RESETn

FX3 additional connections

For configuration purposes some additional connections between Xilinx™ FPGA and Cypress™ EZ-USB FX3 are necessary. The following chart gives some information about these and where to find them on the expansion connector J1.
Additionally GPIO55 and GPIO56 of Cypress™ EZ-USB FX3 are routed to the expansion connector J2. However with EFM-02B default firmware those GPIO signals are not implemented. Please refer to the EZ-USB FX3's data sheet on Cypress™ website for more information about usability of GPIO signals.

FX3	Expansion Connector	FPGA Pin	FPGA Direction	Comment
GPIO45	--	--	--	USB_CONFIGn[9]
GPIO50	--	AB20[10]	Input	FPGA_CSI_B
GPIO51	J1, Pin10	Y22	Output[11]	Done[12]
GPIO52	J1, Pin4	T6	Input/Output[11]	Init_B[12]
GPIO53	J1, Pin8	AA1	Input	Program_B[12]
GPIO54	J2, Pin24	AB19	Input	FPGA_RESETn[12]
GPIO55	J2, Pin19	--	--	FX3 GPIO
GPIO56	J2, Pin21	--	--	FX3 GPIO
GPIO57	--	--	--	FPGA power enable[13]

9 A logic HIGH level enables FGPA configuration via USB. SPI flash clock MUST be set to tri-state mode prior to enabling USB configuration mode.
10 Connected only when FPGA configuration via USB is enabled.
11 Open drain.
12 Pull-up resistor connected onboard EFM-02B.
13 A logic HIGH level enables FPGA power supplies. See EFM-02B power supply options for more details.

Expansion connectors

Two 0,80mm 120-pin Q Strip high-speed ground plane expansion connectors (Samtec™: QSE-060-01-L-D-A) on the bottom-side of the EFM-02B offer access to up to 191 FPGA I/O, three FX3 GPIO, FX3 I²C interface, FX3 and Spartan-6 JTAG signals, some configuration I/O and power rails. Optionally USB signals are available. As default all I/O are configured for 3,3V LVTTL signaling levels. Optionally VCCO power supplies for bank 0 and bank 1 of the Spartan-6 FPGA can be accessed independently. Then an adequate power supply has to be connected to the corresponding expansion pins to set the required signaling level.[14]

Samtec™ offers mating connectors in several variations resulting in different total mating heights. See the following table for some information. Please refer to the Samtec™ website for details.

Samtec™ part number	Mated height
QTE-060-01-L-D	5.00mm
QTE-060-02-L-D	8.00mm
QTE-060-03-L-D	11.00mm
QTE-060-04-L-D	16.00mm
QTE-060-05-L-D	19.00mm
QTE-060-07-L-D	25.00mm

14 Independent access to VCCO power supplies for bank 0 and bank 1 requires special assembly option. Do not connect any power supply to these pins with default EFM-02B modules. This will damage EFM-02B or connected electronics.

Pinout expansion connector J1

J1 - odd								J1 - even							
Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45	Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45
1	BL	2	FPGA I/O	L60N2	R7			2	N/A	N/A	FX3 32kHz clock in	FX3_CLKIN32			
3	BL	2	FPGA I/O	L60P2	T7			4	N/A	2	FPGA configuration	Init_B			
5	BL	2	FPGA I/O	L53N2	Y6	N/A		6	Inhibit FPGA configuration from flash[15]			Flash_Inhibit_n			
7	BL	2	FPGA I/O	L53P2	W6	N/A		8	N/A	2	FPGA configuration	Program_B			
9	BL	2	FPGA I/O	L47P2	W9			10	N/A	2	FPGA configuration	Done			
11	BL	2	FPGA I/O	L47N2	Y8			12	BL	2	FPGA I/O	L50P2	U9		
13	N/A	3	1,8V power output	**1.8V**[16]				14	BL	2	FPGA I/O	L46P2	W8		
15	N/A	3	1,8V power output	**1.8V**[16]				16	BL	2	FPGA I/O	L46N2	V7		
17	TL	0	FPGA I/O	L18N0	H11		N/A	18	BL	2	FPGA I/O	L54N2	AB5	N/A	
19	TL	0	FPGA I/O	L18P0	G11		N/A	20	BL	2	FPGA I/O	L54P2	Y5	N/A	
21	TL	0	FPGA I/O - GCLK	L34N0 - GCLK18	A10			22	BL	2	FPGA I/O	L63N2	V5		
23	TL	0	FPGA I/O - GCLK	L34P0 - GCLK19	B10			24	BL	2	FPGA I/O	L63P2	U6		
25	TL	0	FPGA I/O	L33P0	D10			26	BL	2	FPGA I/O	L59N2	R8		
27	TL	0	FPGA I/O	L33N0	C10			28	BL	2	FPGA I/O	L59P2	R9		
29	TL	0	FPGA I/O	L6P0	B8			30	TL	0	FPGA I/O	L5P0	C7		
31	TL	0	FPGA I/O	L6N0	A8			32	TL	0	FPGA I/O	L5N0	A7		
33	TR	0	FPGA I/O	L45P0	F13		N/A	34	TL	0	FPGA I/O	L8P0	C9		
35	TR	0	FPGA I/O	L45N0	D13		N/A	36	TL	0	FPGA I/O - VREF	L8N0	A9		
37	TR	0	FPGA I/O - GCLK	L36P0 - GCLK15	D11			38	TR	0	FPGA I/O	L44P0	H12		N/A
39	TR	0	FPGA I/O - GCLK	L36N0 - GCLK14	C12			40	TR	0	FPGA I/O	L44N0	F12		N/A

15 Default FPGA configuration at startup is from SPI flash. To prevent SPI configuration, drive this pin to a logic LOW level, prior to enabling FPGA power supplies.
16 On-board 1A switching power supply output. Also supplies FPGA bank 3 and DDR2 memory device.

J1 - odd								J1 - even							
Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45	Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45
41	TR	0	FPGA I/O - VREF	L38N0	A13			42	TL	0	FPGA I/O	L3P0	D6		
43	TR	0	FPGA I/O	L38P0	C13			44	TL	0	FPGA I/O	L3N0	C6		
45	TR	0	FPGA I/O	L50N0	A14			46	TL	0	FPGA I/O	L32P0	D7		
47	TR	0	FPGA I/O	L50P0	B14			48	TL	0	FPGA I/O	L32N0	D8		
49	TR	0	FPGA I/O	L46P0	H13		N/A	50	TL	0	FPGA I/O	L7N0	C8		
51	TR	0	FPGA I/O	L46N0	G13		N/A	52	TL	0	FPGA I/O	L7P0	D9		
53	TR	0	FPGA I/O	L43P0	E12		N/A	54	TL	0	FPGA I/O	L14P0	E8		N/A
55	TR	0	FPGA I/O	L43N0	D12		N/A	56	TL	0	FPGA I/O	L14N0	F8		N/A
57	TR	0	FPGA I/O	L49P0	D14			58	TL	0	FPGA I/O	L2N0	A5		
59	TR	0	FPGA I/O	L49N0	C14			60	TL	0	FPGA I/O	L2P0	C5		
61	TR	0	FPGA I/O	L51N0	A15			62	TL	0	FPGA I/O	L16N0	H10		N/A
63	TR	0	FPGA I/O	L51P0	C15			64	TL	0	FPGA I/O	L16P0	G9		N/A
65	TL	0	FPGA I/O - GCLK	L35P0 - GCLK17	C11			66	BL	2	FPGA I/O	L40N2	T11		
67	TL	0	FPGA I/O - GCLK	L35N0 - GCLK16	A11			68	BL	2	FPGA I/O	L40P2	R11		
69	TR	0	FPGA I/O	L48P0	F14		N/A	70	TL	0	FPGA I/O	L15P0	G8		N/A
71	TR	0	FPGA I/O	L48N0	H14		N/A	72	TL	0	FPGA I/O	L15N0	F9		N/A
73	TR	0	FPGA I/O - SCP	L63N0 - SCP6[17]	A16			74	TL	0	FPGA I/O	L4N0	A6		
75	TR	0	FPGA I/O - SCP	L63P0 - SCP7[17]	B16			76	TL	0	FPGA I/O	L4P0	B6		
77	TR	0	FPGA I/O - VREF	L62N0	C16			78	TL	0	FPGA I/O	L17P0	E10		N/A
79	TR	0	FPGA I/O	L62P0	D15			80	TL	0	FPGA I/O	L17N0	F10		N/A

17 Dual purpose FPGA I/O signals. SCP pins are activated based on suspend setting.

J1 - odd								J1 - even							
Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45	Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45
81	TR	0	FPGA I/O - SCP	L66P0 - SCP1[18]	E16			82	N/A	0	Bank 0 power	**VCCO_IO0**[19]			
83	TR	0	FPGA I/O - SCP	L66N0 - SCP0[18]	D17			84	N/A	0	Bank 0 power	**VCCO_IO0**[19]			
85	RT	1	FPGA I/O	L20P1	A20			86	TL	0	FPGA I/O	L1P0[20]	A3		
87	RT	1	FPGA I/O	L20N1	A21			88	TL	0	FPGA I/O - VREF	L1N0	A4		
89	TR	0	FPGA I/O - SCP	L64N0 - SCP4[18]	A17			90	TR	0	FPGA I/O	L47N0	F15		N/A
91	TR	0	FPGA I/O - SCP	L64P0 - SCP5[18]	C17			92	TR	0	FPGA I/O	L47P0	E14		N/A
93	RT	1	FPGA I/O	L9P1	G16			94	TR	0	FPGA I/O - GCLK	L37P0 - GCLK13	B12		
95	RT	1	FPGA I/O	L9N1	G17			96	TR	0	FPGA I/O - GCLK	L37N0 - GCLK12	A12		
97	RT	1	FPGA I/O	L10P1	F16			98	RT	1	FPGA I/O	L28P1	H16		
99	RT	1	FPGA I/O	L10N1	F17			100	RT	1	FPGA I/O - VREF	L28N1	H17		
101	TR	0	FPGA I/O - SCP	L65N0 - SCP2[18]	A18			102	RT	1	FPGA I/O	L30P1	F18		
103	TR	0	FPGA I/O - SCP	L65P0 - SCP3[18]	B18			104	RT	1	FPGA I/O	L30N1	F19		
105	RT	1	FPGA I/O	L19P1	B21			106	RT	1	FPGA I/O	L33P1	G19		
107	RT	1	FPGA I/O	L19N1	B22			108	RT	1	FPGA I/O	L33N1	F20		
109	N/A	N/A	FPGA JTAG	TDO	A19			110	RT	1	FPGA I/O	L1P1	C19		
111	N/A	N/A	FPGA JTAG	TMS	C18			112	RT	1	FPGA I/O - VREF	L1N1	B20		
113	N/A	N/A	FPGA JTAG	TCK	G15			114	N/A	2	3,3V power output	**VCCO_3V3**[21]			
115	N/A	N/A	FPGA JTAG	TDI	E18			116	N/A	2	3,3V power output	**VCCO_3V3**[21]			
117	N/A	N/A	FPGA suspend pin	SUSPEND[22]	N15			118	RT	1	FPGA I/O	L32P1	C20		
119	N/A	N/A	FPGA power enable	PWR_ENA_EXT[23]				120	RT	1	FPGA I/O	L32N1	C22		

18 Dual purpose FPGA I/O signals. SCP pins are activated based on suspend setting.
19 Connected to VCCO_3V3 onboard. Assembly option available to access FPGA bank 0 VCCO supply independently to support signal levels other than 3.3V.
20 Dual purpose FPGA I/O. A logic low level enables pre-configuration pull-up resistors. 4.7kOhm resistor to VCCO_IO0 connected onboard.
21 On-board 3.3V 3A switching power supply output. Also supplies FPGA bank 2, VCCAUX and JTAG.
22 Optional FPGA suspend feature input pin. On-board 4.7kOhm pull-down resistor. Please see Xilinx™ documentation for more details.

Pinout expansion connector J2

J2 - odd							J2 - even						
Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45	Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45
1	N/A	N/A	5V power input	**VBUS_IO**[24]				2	N/A	N/A	USB2.0 D-	SS_DM[26]			
3	N/A	N/A	5V power input	**VBUS_IO**[24]				4	N/A	N/A	USB2.0 D+	SS_DP[26]			
5	N/A	N/A	5V power output	**VBUS_CON**[25]				6	N/A	N/A	USB OTG ID	OTG_ID[26]			
7	N/A	N/A	USB3.0 TX-	SS_TX_M[26]				8	N/A	N/A	FX3 JTAG	FX3_TRSTn			
9	N/A	N/A	USB3.0 TX+	SS_TX_P[26]				10	N/A	N/A	FX3 JTAG	FX3_TDO			
11	N/A	N/A	USB3.0 RX+	SS_RX_P[26]				12	N/A	N/A	FX3 JTAG	FX3_TMS			
13	N/A	N/A	USB3.0 RX-	SS_RX_M[26]				14	N/A	N/A	FX3 JTAG	FX3_TDI			
15	N/A	N/A	FX3 I²C power	**FX3_VIO5**[27]				16	N/A	N/A	FX3 Reset input	FX3_RESETn			
17	N/A	N/A	FX3 JTAG	FX3_TCK				18	N/A	N/A	FX3 I²C data I/O	FX3_SDA			
19	N/A	N/A	FX3 I/O	FX3_GPIO55				20	N/A	N/A	FX3 I2C clock output	FX3_SCL			
21	N/A	N/A	FX3 I/O	FX3_GPIO56				22	N/A	N/A	Not connected				
23	N/A	N/A	Not connected					24		2	FX3_GPIO54	FPGA_RESETn	AB19		
25	BL	2	FPGA I/O	L52P2	T10	N/A		26	BR	2	FPGA I/O	L18N2	W13		
27	BL	2	FPGA I/O	L52N2	U10	N/A		28	BR	2	FPGA I/O	L18P2	V13		
29	BL	2	FPGA I/O	L51N2	U8	N/A		30	BR	2	FPGA I/O	L22N2	U12	N/A	
31	BL	2	FPGA I/O	L51P2	T8	N/A		32	BR	2	FPGA I/O	L22P2	T12	N/A	
33	BR	2	FPGA I/O	L20N2	Y14			34	BR	2	FPGA I/O	L23P2	T14		

23 Internal logic controls FPGA power supplies. If FPGA power supplies need to be enabled regardless of USB connection status, drive this pin to a logic HIGH level (LVTTL 3.3V) or connect to VBUS_IO.
24 EFM-02B power supply input. Either connect VBUS_CON or an adequate 5.0V power supply.
25 Directly connected to USB3.0 VBUS power supply through a ferrite bead.
26 Reserved. Requires special assembly option. See ordering information for more details.
27 On-board 3.3V 1A switching power supply output. Also supplies EZ-FX3 VIO and I²C EEPROM.

J2 - odd								J2 - even							
Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45	Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45
35	BR	2	FPGA I/O	L20P2	W14			36	BR	2	FPGA I/O	L23N2	R13		
37	BL	2	FPGA I/O	L44N2	Y10			38	BR	2	FPGA I/O	L9N2	V18		
39	BL	2	FPGA I/O	L44P2	W10			40	BR	2	FPGA I/O	L9P2	V19		

J2 - odd								J2 - even							
Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45	Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45
41	BL	2	FPGA I/O - GCLK	L32P2 - GCLK29	Y11			42	RB	1	FPGA I/O	L59P1	P19		
43	BL	2	FPGA I/O - GCLK	L32N2 - GCLK28	AB11			44	RB	1	FPGA I/O	L59N1	P20		
45	BR	2	FPGA I/O	L8N2	U16			46	RB	1	FPGA I/O	L51N1	U22		
47	BR	2	FPGA I/O	L8P2	U17			48	RB	1	FPGA I/O	L51P1	U20		
49	RB	1	FPGA I/O	L74N1	T20			50	RB	1	FPGA I/O	L58P1	M16		
51	RB	1	FPGA I/O - AWAKE	L74P1[28]	T19			52	RB	1	FPGA I/O	L58N1	L15		
53	RB	1	FPGA I/O	L73N1	R19			54	RT	1	FPGA I/O	L34N1	H18		
55	RB	1	FPGA I/O	L73P1	P18			56	RT	1	FPGA I/O	L34P1	H19		
57	BR	2	FPGA I/O	L17N2	W15	N/A		58	RT	1	FPGA I/O	L36N1	K17		
59	BR	2	FPGA I/O	L17P2	Y16	N/A		60	RT	1	FPGA I/O	L36P1	J17		
61	N/A	N/A	1.2V power output	**VCCINT_1V2**[29]				62	BR	2	FPGA I/O	L10P2	R16		
63	N/A	N/A	1.2V power output	**VCCINT_1V2**[29]				64	BR	2	FPGA I/O	L10N2	R15		
65	RB	1	FPGA I/O - VREF	L53N1	N19			66	RB	1	FPGA I/O	L72P1	P17		
67	RB	1	FPGA I/O	L53P1	M19			68	RB	1	FPGA I/O	L72N1	N16		
69	RB	1	FPGA I/O	L60P1	W20			70	RB	1	FPGA I/O	L71P1	M17		
71	RB	1	FPGA I/O	L60N1	W22			72	RB	1	FPGA I/O	L71N1	M18		
73	RB	1	FPGA I/O	L70N1	V20			74	RB	1	FPGA I/O	L61N1	K18		
75	RB	1	FPGA I/O	L70P1	U19			76	RB	1	FPGA I/O	L61P1	L17		
77	RB	1	FPGA I/O - GCLK	L42N1 - GCLK6	L19			78	RT	1	FPGA I/O	L21P1	K16		
79	RB	1	FPGA I/O - GCLK	L42P1 - GCLK7	M20			80	RT	1	FPGA I/O	L21N1	J16		

28 Dual purpose FPGA I/O signal. Awake pin is activated based on suspend setting.
29 On-board 1.2V 1A switching power supply output. Also supplies FPGA VCCINT.

J2 - odd								J2 - even							
Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45	Pin	BUFIO2 Region	FPGA Bank	Description	Signal	LX150	LX100	LX45
81	BR	2	GCLK - USERCCLK	USERCCLK	AB13			82	RB	1	FPGA I/O	L52P1	V21		
83	AES key memory power supply input			VBATT	R17		N/A	84	RB	1	FPGA I/O	L52N1	V22		
85	BR	2	100MHz clock	SYSCLK	W12			86	RB	1	FPGA I/O	L50P1	T21		
87	AES key EFUSE power supply input			VFS	P16		N/A	88	RB	1	FPGA I/O	L50N1	T22		
89	RB	1	FPGA I/O	L49P1	R20			90	RB	1	FPGA I/O - HDC[30]	L48P1	P21		
91	RB	1	FPGA I/O	L49N1	R22			92	RB	1	FPGA I/O	L48N1	P22		
93	RB	1	FPGA I/O	L47P1	N20			94	RB	1	FPGA I/O	L46P1	M21		
95	RB	1	FPGA I/O - LDC[31]	L47N1	N22			96	RB	1	FPGA I/O	L46N1	M22		
97	RT	1	FPGA I/O - GCLK	L40P1 - GCLK11	K20			98	RB	1	FPGA I/O	L45N1	L22		
99	RT	1	FPGA I/O - GCLK	L40N1 - GCLK10	K19			100	RB	1	FPGA I/O	L45P1	L20		
101	RB	1	FPGA I/O - GCLK	L43P1 - GCLK5	J20			102	RB	1	FPGA I/O	L44P1	K21		
103	RB	1	FPGA I/O - GCLK	L43N1 - GCLK4	J22			104	RB	1	FPGA I/O	L44N1	K22		
105	RT	1	FPGA I/O	L38N1	J19			106	RT	1	FPGA I/O - GCLK	L41P1 - GCLK9	H21		
107	RT	1	FPGA I/O	L38P1	H20			108	RT	1	FPGA I/O - GCLK	L41N1 - GCLK8	H22		
109	RT	1	FPGA I/O	L39N1	G22			110	RT	1	FPGA I/O	L37P1	F21		
111	RT	1	FPGA I/O	L39P1	G20			112	RT	1	FPGA I/O	L37N1	F22		
113	RT	1	FPGA I/O	L35N1	E22			114	RT	1	FPGA I/O	L31P1	D21		
115	RT	1	FPGA I/O	L35P1	E20			116	RT	1	FPGA I/O	L31N1	D22		
117	RT	1	FPGA I/O	L29P1	D19			118	N/A	1	Bank 1 power	**VCCO_IO1**[32]			
119	RT	1	FPGA I/O	L29N1	D20			120	N/A	1	Bank 1 power	**VCCO_IO1**[32]			

30 High during configuration.
31 Low during configuration.
32 Connected to VCCO_3V3 onboard. Assembly option available to access FPGA bank 1 VCCO supply independently to support signal levels other than 3,3V. See ordering information for more details.

Breakout board

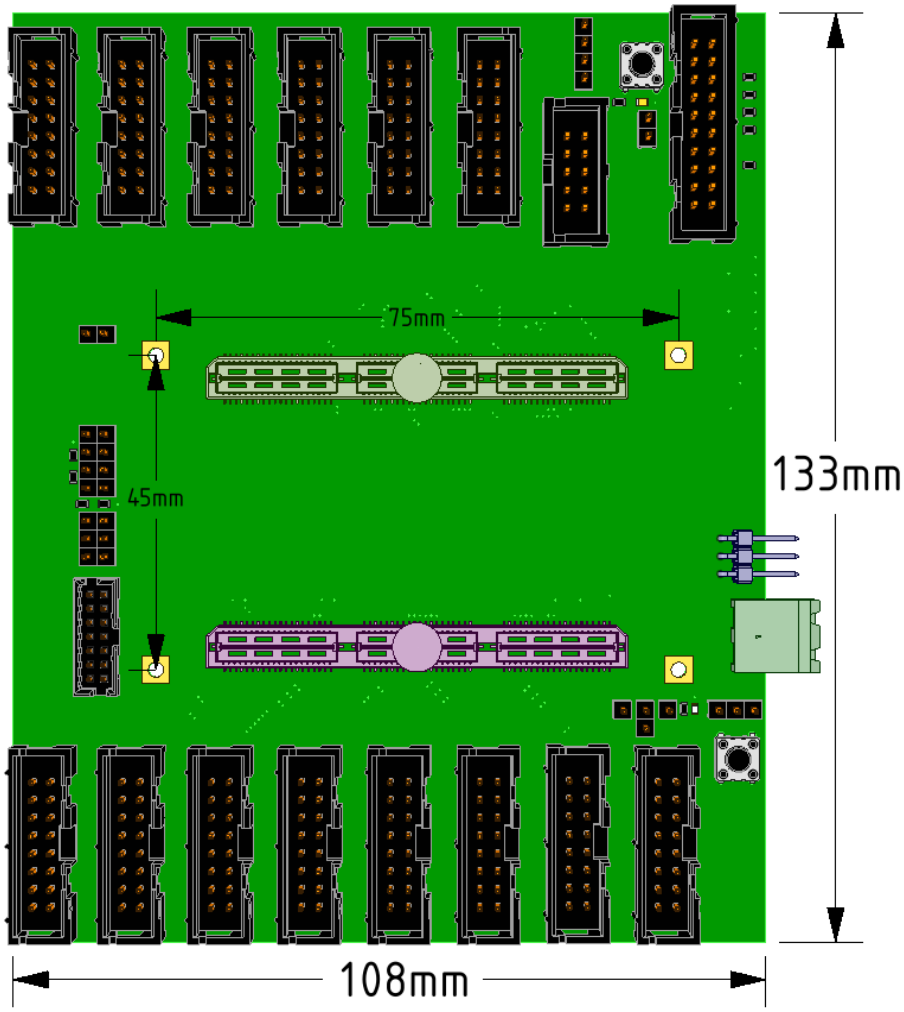


Figure 6: EFM-02B breakout board

To simplify connecting to IOs on the expansion connectors J1 and J2 of EFM-02B modules during evaluation process the EFM-02B breakout board is available. This two-layer board provides access to all FPGA IOs and EZ-USB FX3 GPIOs and I²C interface through standard 2,54mm through-hole connectors. Standard connectors for FPGA and EZ-USB FX3 JTAG are available as well as push-buttons for FPGA Program_B and EZ-USB FX3 reset. Jumpers are provided to enable FPGA suspend mode or flash inhibit functionality and select between the various power supply options of the EFM-02B module - bus-powered or self-powered, with or without power supply sequencing. To connect an external 5,0V power supply, a 2-pin 5,08mm connector is provided.

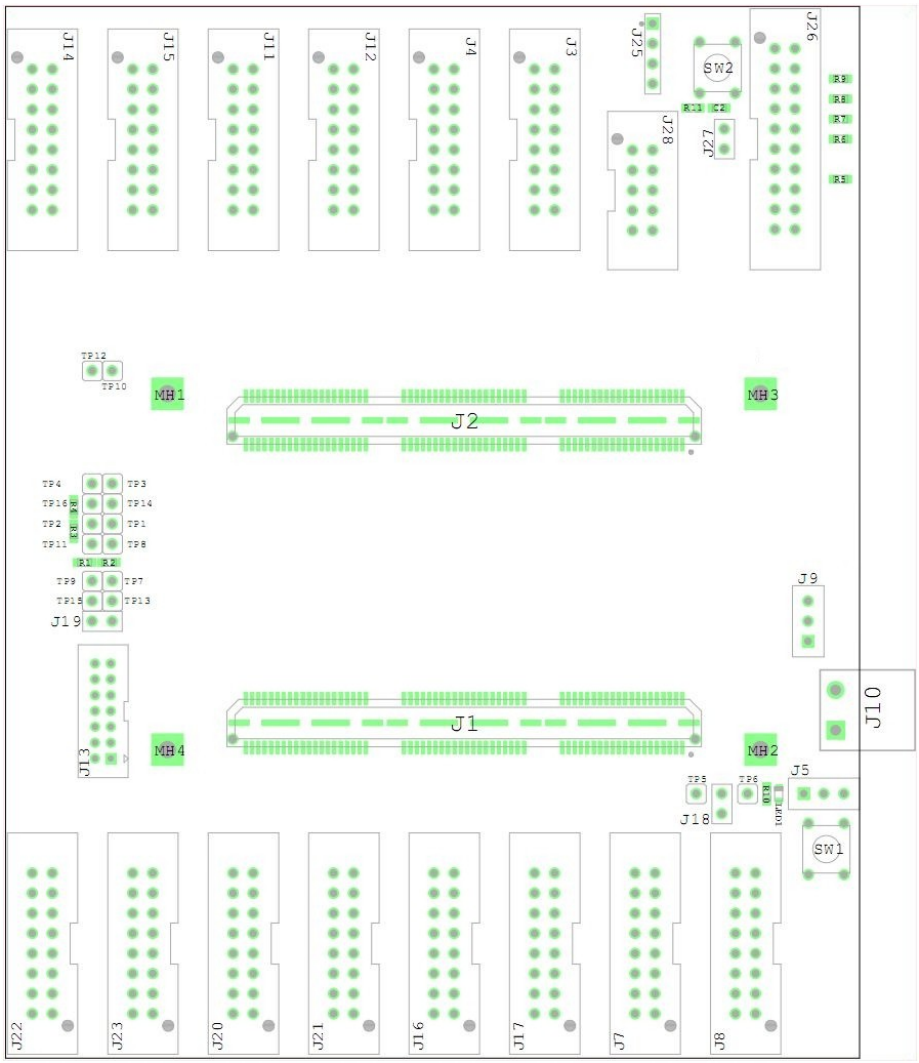


Figure 7: EFM-02B breakout board connectors

Power supply options

The EFM-02B breakout board supports all power supply options of the EFM-02B modules. Connectors J5 and J9 are used to select the appropriate power scheme. J10 serves as input for an optional external 5,0V power supply.

J5 - FPGA power on sequence select		
Jumper Position	**Power on sequence**	**Comment**
1-2	USB- controlled	
2-3	Instant on	Requires self-powered mode

J9 - Power source select		
Jumper Position	**Power scheme**	**Power supply**
1-2	Bus-powered	USB 5,0V VBUS
2-3	Self-powered	External 5,0V at J10

J10 - External power supply input		
Pin	**Signal**	**Comment**
1	GND	Negative terminal for external power supply
2	5V_EXT	Positive terminal for external 5,0V power supply

External power supply input requirements				
	Min.	**Typ.**	**Max.**	**Units**
Power supply input range	4,5	5	5,5	V
Minimum current requirement[33]		650		mA

33 XC6SLX150-3FGG484I, UDK3PerfMon (efm02_soc_top_xc6slx150.bin) @ maximum USB3.0 data rate.

JTAG and push-buttons

With the 14-pin 2mm connector J13 the EFM-02B breakout board supports standard Xilinx™ JTAG download cables to connect to the Xilinx™ Spartan-6 device. With the help of the free Xilinx™ ISE WebPack the FPGA and the attached SPI flash can be programmed using the iMPACT programming software. Please refer to the application note XAPP586 and the Spartan-6 configuration user guide UG380 for further details. Once the SPI flash is programmed with a valid bitstream, reprogramming of the FPGA can be initiated by pressing the push-button SW1.

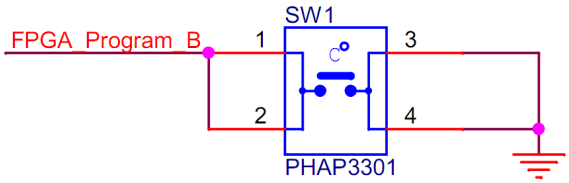


Figure 10: SW1 - FPGA Program_B

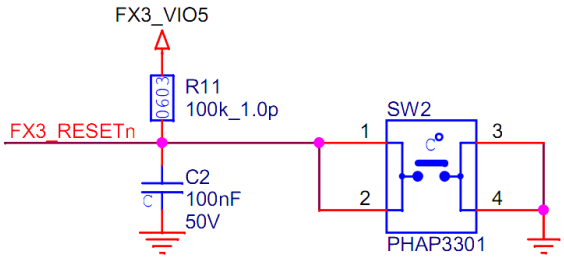


Figure 9: SW2 - EZ-FX3 Reset

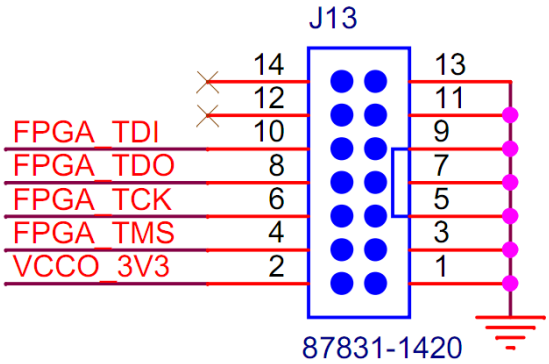


Figure 8: J13 - FPGA JTAG

Additionally the EZ-USB FX3 JTAG interface is routed to J26, a standard 2,54mm 20-pin shrouded header. This allows direct connection of the JTAG/SWD Emulator with USB interface from Segger, which is recommended by Cypress™. For more details please refer to the FX3 Programmers Manual within EZ-USB FX3 Software Development Kit. To hard reset EZ-USB FX3 press the push-button SW2.

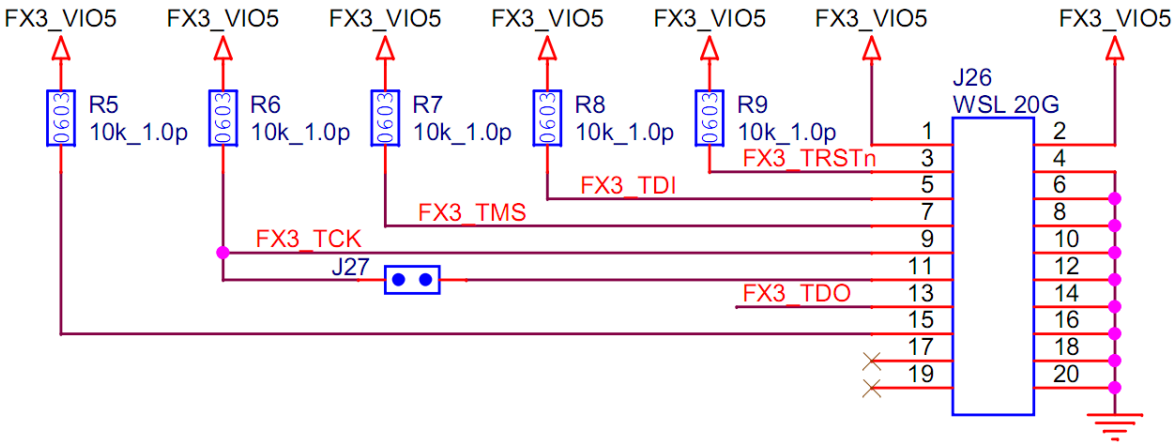


Figure 11: J26 - EZ-USB FX3 JTAG

EZ-USB FX3 GPIO and I²C

The general purpose inputs/outputs GPIO55 and GPIO56 of the Cypress™ EZ-USB FX3 controller are available at the shrouded header J28. The optionally usable watchdog timer inside FX3 may be optionally supplied by an external 32-kHz clock source. The associated CLKIN32 input is accessible at pin three of connector J28.

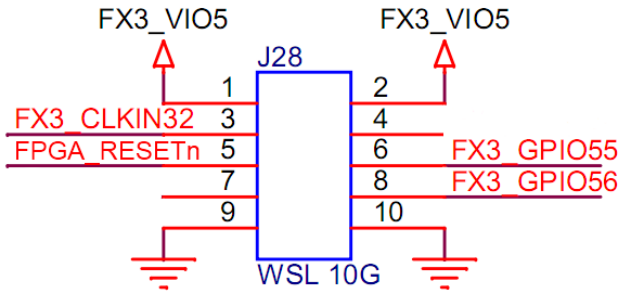


Figure 12: FX3 GPIO signals

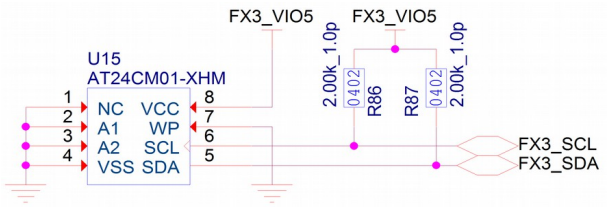


Figure 13: EZ-USB FX3 I²C EEPROM on EFM-02B module

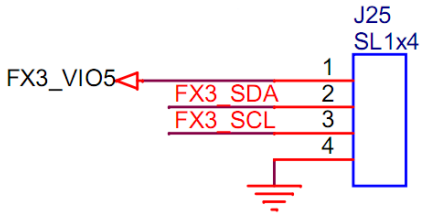


Figure 14: J25 - EZ-USB FX3 I²C connector

EFM-02B uses the I²C EEPROM AT24CM01-XHM from Atmel to store VID/PID data. To increase available storage for larger firmware files EZ-USB FX3 supports multiple devices of the same size and type sharing the I²C bus. On more information about boot options using the I²C interface please consult AN76405 from Cypress™.

FPGA input-output- signals

Except IO 'L50P2' (FPGA ball U9) located at pin 12 of the EFM-02B expansion connector J1, which is connected to the green led LED1 onboard the EFM-02B breakout board, all other FPGA IO signals are routed to standard 2,54mm through-hole shrouded headers. Additionally jumpers are provided for Flash_Inhibit_n and FPGA_SUSPEND together with test pins for several FPGA supply voltages and status signals.

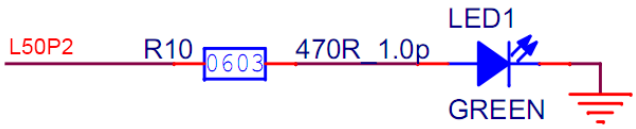


Figure 15: LED1

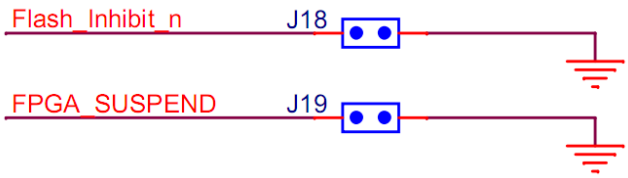


Figure 16: Jumpers for SUSPEND and Flash_Inhibit_n

Figure 17: VFS

Figure 18: VBATT

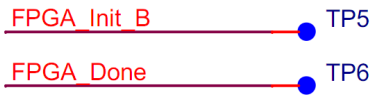


Figure 19: InitB, Done

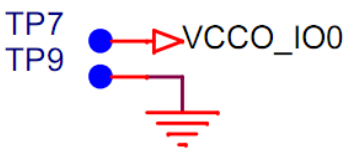


Figure 20: VCCO_IO0

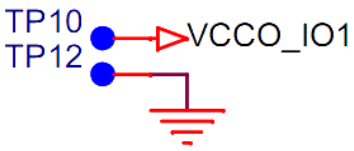


Figure 21: VCCO_IO1

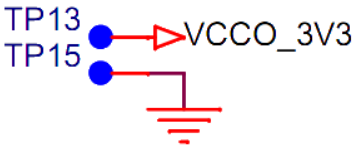


Figure 22: VCCO_3V3

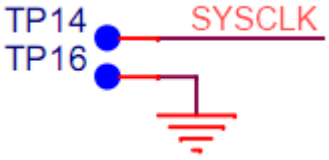


Figure 23: SYSCLK

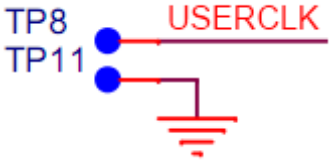


Figure 24: USERCLK

J14 - odd					J14 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L73N1	R19	J2, 53	BANK1 OPT IO17	**2**	L73P1	P18	J2, 55	BANK1 OPT IO16
3	L41N1	H22	J2, 108	BANK1 IO31	**4**	L41P1	H21	J2, 106	BANK1 IO30
5	L37N1	F22	J2, 112	BANK1 IO23	**6**	L37P1	F21	J2, 110	BANK1 IO22
7	L31N1	D22	J2, 116	BANK1 IO11	**8**	L31P1	D21	J2, 114	BANK1 IO10
9	L29P1	D19	J2, 117	BANK1 IO6	**10**	L29N1	D20	J2, 119	BANK1 IO7
11	L35N1	E22	J2, 113	BANK1 IO19	**12**	L35P1	E20	J2, 115	BANK1 IO18
13	L39N1	G22	J2, 109	BANK1 IO27	**14**	L39P1	G20	J2, 111	BANK1 IO26
15	**GND**			**Power**	**16**	**GND**			**Power**

J15 - odd					J15 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L70P1	V20	J2, 73	BANK1 OPT IO11	**2**	L70N1	U19	J2, 75	BANK1 OPT IO10
3	L52N1	V22	J2, 84	BANK1 IO53	**4**	L52P1	V21	J2, 82	BANK1 IO52
5	L50N1	T22	J2, 88	BANK1 IO49	**6**	L50P1	T21	J2, 86	BANK1 IO48
7	L48N1	P22	J2, 92	BANK1 IO45	**8**	L48P1[34]	P21	J2, 90	BANK1 IO44
9	L46N1	M22	J2, 96	BANK1 IO41	**10**	L46P1	M21	J2, 94	BANK1 IO40
11	L45P1	L20	J2, 100	BANK1 IO38	**12**	L45N1	L22	J2, 98	BANK1 IO39
13	L44N1	K22	J2, 104	BANK1 IO37	**14**	L44P1	K21	J2, 102	BANK1 IO36
15	**GND**			**Power**	**16**	**GND**			**Power**

J11 - odd					J11 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L53N1	N19	J2, 65	BANK1 IO55	**2**	L53P1	M19	J2, 67	BANK1 IO54
3	L71N1	M18	J2, 72	BANK1 OPT IO13	**4**	L71P1	M17	J2, 70	BANK1 OPT IO12
5	L60P1	W20	J2, 69	BANK1 IO58	**6**	L60N1	W22	J2, 71	BANK1 IO59
7	L42N1	L19	J2, 77	BANK1 IO33	**8**	L42P1	M20	J2, 79	BANK1 IO32
9	**1,2V**		J2, 63	**1,2V power output**	**10**	**1,2V**		J2, 61	**1,2V power output**
11	L21N1	J16	J2, 80	BANK1 OPT IO5	**12**	L21P1	K16	J2, 78	BANK1 OPT IO4
13	L61P1	L17	J2, 76	BANK1 IO60	**14**	L61N1	K18	J2, 74	BANK1 IO61
15	**GND**			**Power**	**16**	**GND**			**Power**

34 High during configuration.

J12 - odd					J12 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L51P1	U20	J2, 48	BANK1 IO50	**2**	L51N1	U22	J2, 46	BANK1 IO51
3	L58N1	L15	J2, 52	BANK1 OPT IO9	**4**	L58P1	M16	J2, 50	BANK1 OPT IO8
5	L34P1	H19	J2, 56	BANK1 IO16	**6**	L34N1	H18	J2, 54	BANK1 IO17
7	L36P1	J17	J2, 60	BANK1 IO20	**8**	L36N1	K17	J2, 58	BANK1 IO21
9	L10N2	R15	J2, 64	BANK2 OPT IO5	**10**	L10P2	R16	J2, 62	BANK2 OPT IO4
11	L72N1	N16	J2, 68	BANK1 OPT IO15	**12**	L72P1	P17	J2, 66	BANK1 OPT IO14
13	L74P1[35]	T19	J2, 51	BANK1 IO62	**14**	L74N1	T20	J2, 49	BANK1 IO63
15	**GND**			**Power**	**16**	**GND**			**Power**

J4 - odd					J4 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L20P2	W14	J2, 35	BANK2 OPT IO10	**2**	L20N2	Y14	J2, 33	BANK2 OPT IO11
3	L17P2	Y16	J2, 59	BANK2 OPT2 IO0	**4**	L17N2	W15	J2, 57	BANK2 OPT2 IO1
5	L8P2	U17	J2, 47	BANK2 OPT IO0	**6**	L8N2	U16	J2, 45	BANK2 OPT IO1
7	L44N2	Y10	J2, 37	BANK2 OPT IO17	**8**	L44P2	W10	J2, 39	BANK2 OPT IO16
9	L46N2	V7	J1, 16	BANK2 OPT IO19	**10**	L46P2	W8	J1,14	BANK2 OPT IO18
11	L54P2	Y5	J1, 20	BANK2 OPT2 IO10	**12**	L54N2	AB5	J1,18	BANK2 OPT2 IO11
13	L32N2	AB11	J2, 43	BANK2 IO1	**14**	L32P2	Y11	J2,41	BANK2 IO0
15	**GND**			**Power**	**16**	**GND**			**Power**

J3 - odd					J3 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L18P2	V13	J2, 28	BANK2 OPT IO8	**2**	L18N2	W13	J2, 26	BANK2 OPT IO9
3	L22P3	T12	J2, 32	BANK2 OPT2 IO2	**4**	L22N2	U12	J2, 30	BANK2 OPT2 IO3
5	L23N2	R13	J2, 36	BANK2 OPT IO13	**6**	L23P2	T14	J2, 34	BANK2 OPT IO12
7	L9P2	V19	J2, 40	BANK2 OPT IO2	**8**	L9N2	V18	J2, 38	BANK2 OPT IO3
9	L52N2	U10	J2, 27	BANK2 OPT2 IO7	**10**	L52P2	T10	J2, 25	BANK2 OPT2 IO6
11	L51P2	T8	J2, 31	BANK2 OPT2 IO4	**12**	L51N2	U8	J2, 29	BANK2 OPT2 IO5
13	L59N1	P20	J2, 44	BANK1 IO57	**14**	L59P1	P19	J2, 42	BANK1 IO56
15	**GND**			**Power**	**16**	**GND**			**Power**

35 Dual purpose. AWAKE pin is activated based on suspend setting.

J22 - odd					J22 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L33N1	F20	J1, 108	BANK1 IO15	**2**	L33P1	G19	J1, 106	BANK1 IO14
3	L28N1	H17	J1, 100	BANK1 OPT IO7	**4**	L10P1	F16	J1, 97	BANK1 OPT IO2
5	L38N1	J19	J2, 105	BANK1 IO25	**6**	L38P1	H20	J2,107	BANK1 IO24
7	L43P1	J20	J2, 101	BANK1 IO34	**8**	L43N1	J22	J2,103	BANK1 IO35
9				open	**10**	L28P1	H16	J1, 98	BANK1 OPT IO6
11	L47P1	N20	J2, 93	BANK1 IO42	**12**	L47N1[36]	N22	J2,95	BANK1 IO43
13	L40P1	K20	J2, 97	BANK1 IO28	**14**	L40N1	K19	J2,99	BANK1 IO29
15	**GND**			**Power**	**16**	**GND**			**Power**

J23 - odd					J23 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L1N1	B20	J1, 112	BANK1 IO1	**2**	L1P1	C19	J1, 110	BANK1 IO0
3	L9N1	G17	J1, 95	BANK1 OPT IO1	**4**	L9P1	G16	J1, 93	BANK1 OPT IO0
5	L65N0[37]	A18	J1, 101	BANK0 IO43	**6**	L65P0[37]	B18	J1, 103	BANK0 IO42
7	L19P1	B21	J1, 105	BANK1 IO2	**8**	L19N1	B22	J1, 107	BANK1 IO3
9				open	**10**	L10N1	F17	J1, 99	BANK1 OPT IO3
11	L32P1	C20	J1, 118	BANK1 IO12	**12**	L32N1	C22	J1, 120	BANK1 IO13
13	L49P1	R20	J2, 89	BANK1 IO46	**14**	L49N1	R22	J2,91	BANK1 IO47
15	**GND**			**Power**	**16**	**GND**			**Power**

J20 - odd					J20 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L40N2	T11	J1, 66	BANK2 OPT IO15	**2**	L17N0	F10	J1, 80	BANK0 OPT IO7
3	L20P1	A20	J1, 85	BANK1 IO4	**4**	L20N1	A21	J1, 87	BANK1 IO5
5	L64N0[37]	A17	J1, 89	BANK0 IO41	**6**	L64P0[37]	C17	J1, 91	BANK0 IO40
7	L1P0[38]	A3	J1, 86	BANK0 IO0	**8**	L1N0	A4	J1, 88	BANK0 IO1
9	L47N0	F15	J1, 90	BANK0 OPT IO19	**10**	L47P0	E14	J1, 92	BANK0 OPT IO18
11	L37P0	B12	J1, 94	BANK0 IO26	**12**	L37N0	A12	J1, 96	BANK0 IO27
13	L30P1	F18	J1, 102	BANK1 IO8	**14**	L30N1	F19	J1, 104	BANK1 IO9
15	**GND**			**Power**	**16**	**GND**			**Power**

36 Low during configuration.
37 Dual purpose. SCP pins are activated based on suspend setting.
38 Dual purpose. A logic low enables pre-configuration pull-up resistors. 4,7kOhm resistor to VCCO_IO0.

J21 - odd					J21 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L40P2	R11	J1, 68	BANK2 OPT IO14	**2**	L17P0	E10	J1, 78	BANK0 OPT IO6
3	L63N0[39]	A16	J1, 73	BANK0 IO39	**4**	L63P0[39]	B16	J1, 75	BANK0 IO38
5	L62N0	C16	J1, 77	BANK0 IO37	**6**	L62P0	D15	J1, 79	BANK0 IO36
7	L4P0	B6	J1, 76	BANK0 IO6	**8**	L4N0	A6	J1, 74	BANK0 IO7
9	L15N0	F9	J1, 72	BANK0 OPT IO3	**10**	L15P0	G8	J1, 70	BANK0 OPT IO2
11	L7P0	D9	J1, 52	BANK0 IO12	**12**	L7N0	C8	J1, 50	BANK0 IO13
13	L66P0[39]	E16	J1, 81	BANK0 IO44	**14**	L66N0[39]	D17	J1, 83	BANK0 IO45
15	**GND**			**Power**	**16**	**GND**			**Power**

J16 - odd					J16 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L48P0	F14	J1, 69	BANK0 OPT IO20	**2**	L48N0	H14	J1, 71	BANK0 OPT IO21
3	L14P0	E8	J1, 54	BANK0 OPT IO0	**4**	L14N0	F8	J1, 56	BANK0 OPT IO1
5	L2N0	A5	J1, 58	BANK0 IO3	**6**	L2P0	C5	J1, 60	BANK0 IO2
7	L16N0	H10	J1, 62	BANK0 OPT IO5	**8**	L16P0	G9	J1, 64	BANK0 OPT IO4
9	L35P0	C11	J1, 65	BANK0 IO22	**10**	L35N0	A11	J1, 67	BANK0 IO23
11	L51N0	A15	J1, 61	BANK0 IO35	**12**	L51P0	C15	J1, 63	BANK0 IO34
13	L49P0	D14	J1, 57	BANK0 IO30	**14**	L49N0	C14	J1, 59	BANK0 IO31
15	**GND**			**Power**	**16**	**GND**			**Power**

J17 - odd					J17 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L43P0	E12	J1, 53	BANK0 OPT IO10	**2**	L43N0	D12	J1, 55	BANK0 OPT IO11
3	L46P0	H13	J1, 49	BANK0 OPT IO16	**4**	L46N0	G13	J1, 51	BANK0 OPT IO17
5	L50N0	A14	J1, 45	BANK0 IO33	**6**	L50P0	B14	J1, 47	BANK0 IO32
7	L44N0	F12	J1, 40	BANK0 OPT IO13	**8**	L44P0	H12	J1, 38	BANK0 OPT IO12
9	L32N0	D8	J1, 48	BANK0 IO17	**10**	L32P0	D7	J1, 46	BANK0 IO16
11	L3N0	C6	J1, 44	BANK0 IO5	**12**	L3P0	D6	J1, 42	BANK0 IO4
13	L38N0	A13	J1, 41	BANK0 IO29	**14**	L38P0	C13	J1, 43	BANK0 IO28
15	**GND**			**Power**	**16**	**GND**			**Power**

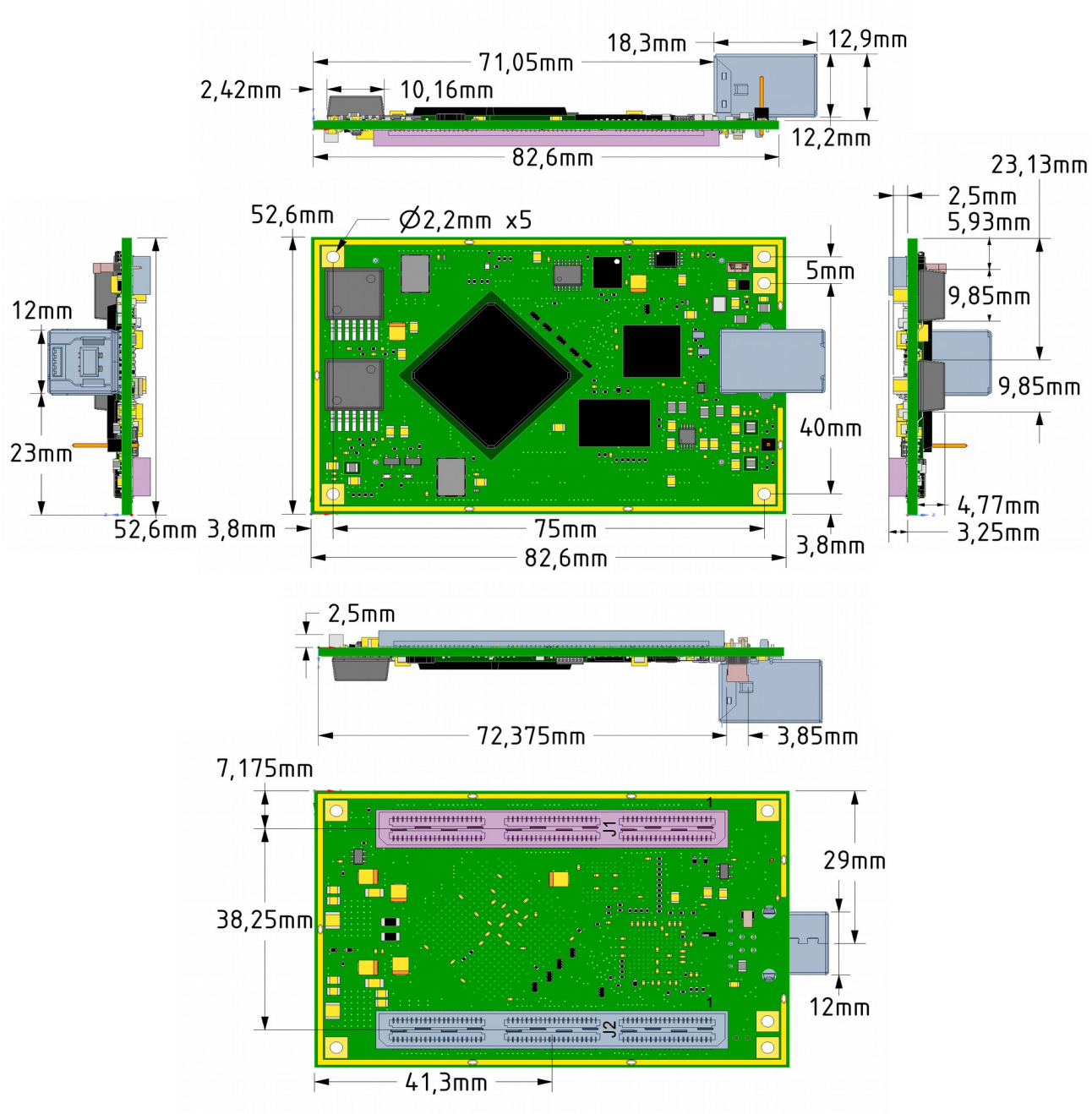
39 Dual purpose. SCP pins are activated based on suspend setting.

J7 - odd					J7 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L60P2	T7	J1, 3	BANK2 OPT IO23	**2**	L60N2	R7	J1, 1	BANK2 OPT IO22
3	L53N2	W6	J1, 7	BANK2 OPT2 IO8	**4**	L53P2	Y6	J1, 5	BANK2 OPT2 IO9
5	L59N2	R8	J1, 26	BANK2 OPT IO25	**6**	L59P2	R9	J1, 28	BANK2 OPT IO24
7	L5P0	C7	J1, 30	BANK0 IO8	**8**	L5N0	A7	J1, 32	BANK0 IO9
9	L8P0	C9	J1, 34	BANK0 IO14	**10**	L8N0	A9	J1, 36	BANK0 IO15
11	L36P0	D11	J1, 37	BANK0 IO24	**12**	L36N0	C12	J1, 39	BANK0 IO25
13	L45P0	F13	J1, 33	BANK0 OPT IO14	**14**	L45N0	D13	J1, 35	BANK0 OPT IO15
15	**GND**			**Power**	**16**	**GND**			**Power**

J8 - odd					J8 - even				
Pin	**Signal**	**Ball**	**Exp.**	**Comment**	**Pin**	**Signal**	**Ball**	**Exp.**	**Comment**
1	L47P2	W9	J1, 9	BANK2 OPT IO20	**2**	L47N2	Y8	J1, 11	BANK2 OPT IO21
3	**1,8V**		J1, 13	**1,8V power output**	**4**	**1,8V**		J1, 15	**1,8V power output**
5	L63N2	V5	J1, 22	BANK2 OPT IO7	**6**	L63P2	U6	J1, 24	BANK2 OPT IO6
7	L6P0	B8	J1, 29	BANK0 IO10	**8**	L6N0	A8	J1, 31	BANK0 IO11
9	L33P0	D10	J1, 25	BANK0 IO18	**10**	L33N0	C10	J1, 27	BANK0 IO19
11	L34N0	A10	J1, 21	BANK0 IO21	**12**	L34P0	B10	J1, 23	BANK0 IO20
13	L18N0	H11	J1, 17	BANK0 OPT IO9	**14**	L18P0	G11	J1, 19	BANK0 OPT IO8
15	**GND**			**Power**	**16**	**GND**			**Power**

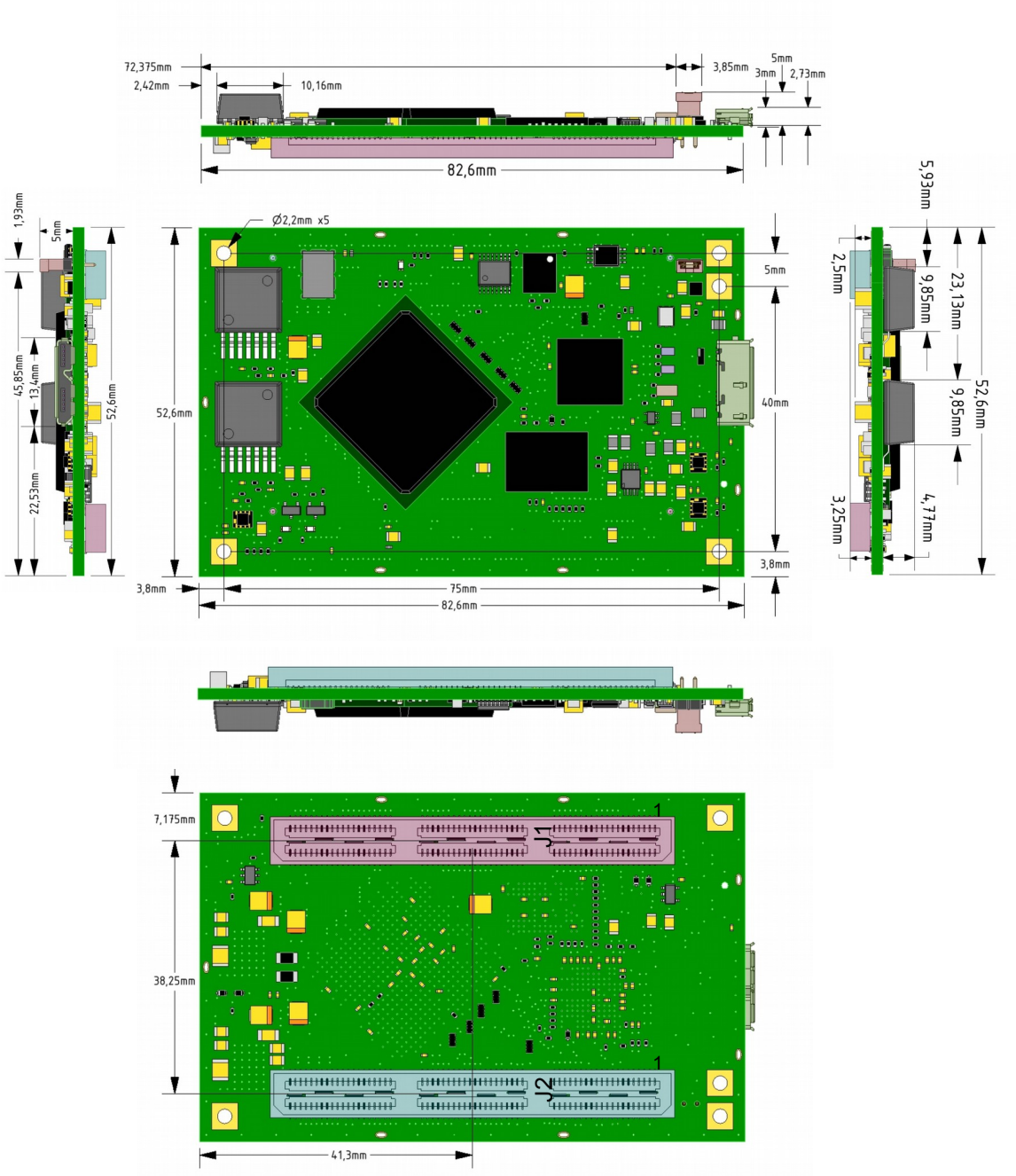
Mechanical drawings

EFM-02B USB Type B connector



The four mounting holes of size M2-fine located in the corners of the PCB are electrically isolated. The fifth mounting hole located next to the USB3.0 type B connector provides access to the USB shielding

EFM-02 USB micro-B connector (obsolete)



The four mounting holes of size M2-fine located in the corners of the PCB are electrically isolated. The fifth mounting hole located next to the USB3.0 type B connector provides access to the USB shielding

EFM-02 / EFM-02B footprint example

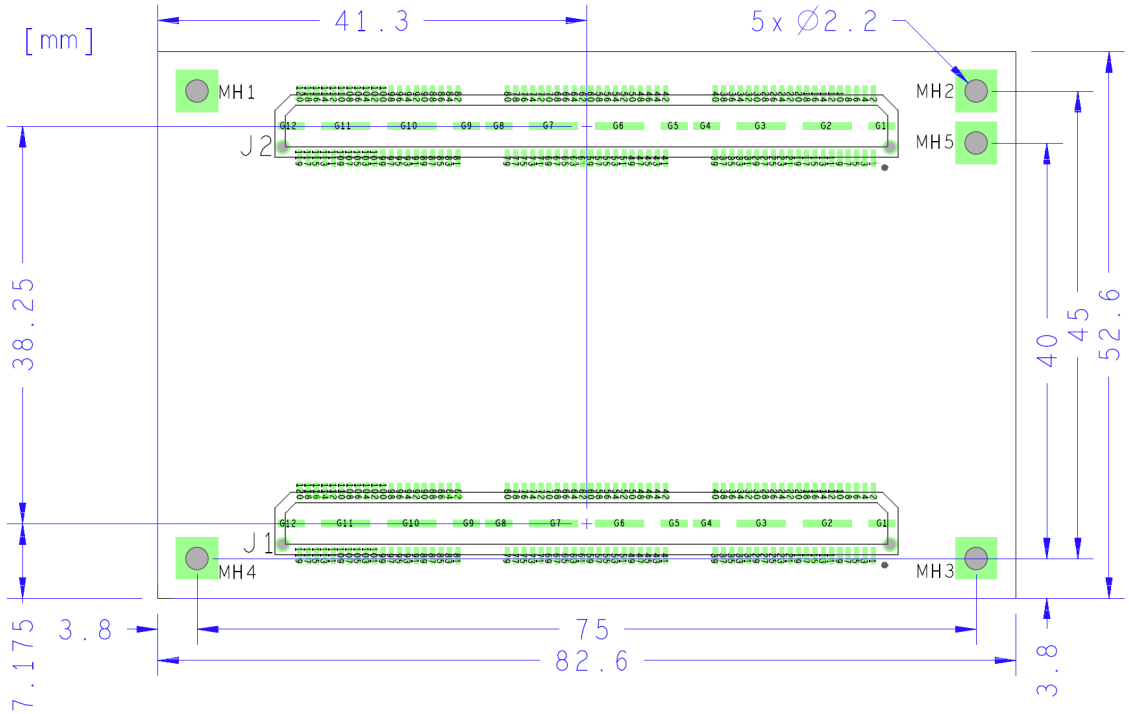


Figure 25: EFM-02 / EFM-02B footprint example

Mating connectors

Samtec™ part number	Mated height
QTE-060-01-L-D	5.00mm
QTE-060-02-L-D	8.00mm
QTE-060-03-L-D	11.00mm
QTE-060-04-L-D	16.00mm
QTE-060-05-L-D	19.00mm
QTE-060-07-L-D	25.00mm

Ordering information

Order Number	FPGA	VCCO Bank 0 / 1	USB3.0 connector	Comment
C028229	XC6SLX45-3FGG484I	VCCO_3V3	Micro-B, on-board	Obsolete
C028239	XC6SLX150-3FGG484I	VCCO_3V3	Micro-B, on-board	Obsolete
C028240	XC6SLX100-3FGG484I	VCCO_3V3	Micro-B, on-board	Obsolete
C028303	XC6SLX150-3FGG484I	VCCO_3V3	Type B, on-board	Standard
C028304	XC6SLX45-3FGG484I	VCCO_3V3	Type B, on-board	Standard

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Revision history

v1.0	Initial release.
v1.1	Improved readability of tables.
	Updates for EFM-02 PCB revision 1.1: EFM02 functional block diagram; PCB size; J4 for onboard bus-powered mode option; SlaveFifo interface; FX3 additional pins; Expansion connector J1, Pins 1, 3, 5, 7, 9, 11, 12, 13, 14, 15, 16, 18, 20, 22, 24; Expansion connector J2, Pins 19, 22, 23, 24; Expansion connector J2, Pins 61 , 63; Breakout board EZ-FX3 GPIO signals; Breakout board LED1; Breakout board J11, Pins 9, 10; Breakout board J4, Pins 7, 8, 9, 10, 11, 12; Breakout board J7, Pins 1, 2, 3, 4; Breakout board J8, Pins 1, 2, 3, 4; EFM02 mechanical drawings; Ordering information;
1.2	Minor updates.
1.3	Updated pin-out of EFM02 breakout board connectors.
1.4	Updated expansion connector J1, Pins 5, 7; Updated expansion connector J2, Pins 37, 39; Updated EFM-02 breakout board connector J4, Pins 7, 8; Updated EFM-02 breakout board connector J7, Pins 3, 4;
1.5	HW Rev 1.2
1.6	Adopted to new layout. Global revision.
1.7	Corrected expansion connector J1, Pins 62, 64; N/A for LX45.
2.0	EFM-02B with USB type B connector replace the obsolete EFM-02 USB micro-B boards.
2.1	Additional information about the footprint for EFM-02 / EFM-02B. Added information about USB2.0 D+/D- lines requirement in default FX-3 USB boot mode.

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