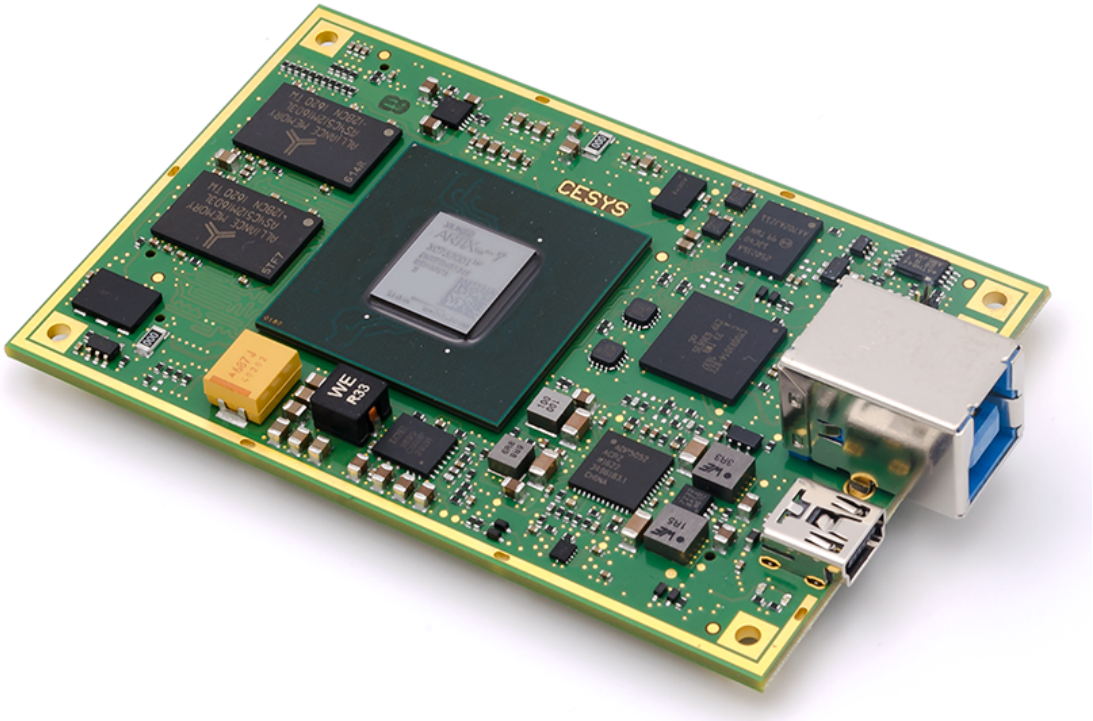
EFM-03
Hardware Reference

(Hardware Revision: Rev. A)



Target applications

- Image processing
- Video capture
- Smart cameras
- High-speed FPGA co-processor
- Custom test equipment

Features

- USB 3.0 SuperSpeed interface through versatile Cypress™ EZ-FX3 controller
- Up to 320 MByte/s sustained data rate
- Industrial grade 7 Series Xilinx™ FPGA XC7A200T-2FBG676I
- 32 MByte Quad-SPI configuration/data memory
- 2 GByte DDR3L, 3.2G Byte/s bandwidth
- USB3.0 Type B connector for highest reliability
- USB bus-powered, no external power supply necessary
- Optional self-powered mode available
- Single 5 V power supply, all necessary power supplies generated onboard by high performance dc/dc converters
- 1 Mbit I²C EEPROM for FX3 configuration data
- I²C interface available on expansion connector to increase available FX3 configuration memory for standalone applications
- Two FX3 GPIO on expansion connector
- 191 single-ended (95 differential) IOs on high-quality high-speed Samtec™ connectors (QSE-060-01), including several clock capable IO
- Independent power supply option for selected FPGA banks
- Two GTP quad columns available on high-quality high-speed Samtec™ connector (QSE-020-01), including 8 TX-, 8 RX- and 4 CLK- pairs
- High performance 200 MHz LVDS clock oscillator
- FPGA configuration from SPI memory, JTAG or USB
- 90 MHz EMCCLK clock oscillator for highest FPGA configuration speeds from flash
- One user, three status leds
- USB 2.0 UART (FTDI FT230X) on USB2.0 mini-B connector for debugging
- JTAG for FPGA and FX3 controller available on expansion connectors
- Small sized PCB only measures 52.6 mm x 82.6 mm
- Pinout and connector positioning compatible[1] to EFM-02/B

1 Additional space on main boards might be required due to additional GTP quad and USB2.0 mini-B connectors on EFM-03.

EFM-03 block diagram

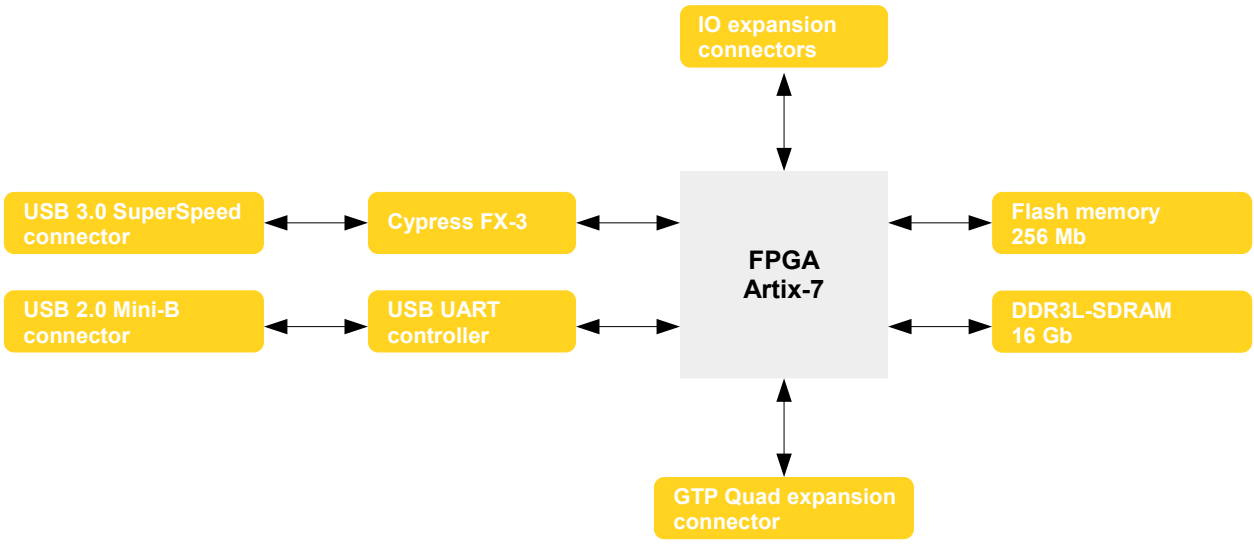


Figure 1: EFM-03 functional block diagram

Specification

Parameter	Min.	Typ.	Max.	Units
Dimensions (B x W)		52.6 x 82.6		mm
Maximum part height on top side besides USB Type B connector		4.3		mm
Maximum part height on bottom side		2.0		mm
Module stacking height[2]	5.0		25.0	mm
Operating temperature range	0		45[3]	°C

2 Depends on mating QTE connector height. Please refer to chapter Digital IO expansion connectors and the Samtec™ website for details.

3 Natural convection cooling. FPGA configured with efm03_wrapper design, USB 3.0 transmission to onboard 2 Gbyte DDR3L memory at maximum speed. Depending on the actual power requirements of the user fpga design, heatsink and/or forced cooling might be required.

FPGA density

Off-the-shelf EFM-03 comes with the Xilinx™ Artix-7 FPGA XC7A200T-2FBG676I. See the following table for some details on this FPGA. For more detailed information please consult Xilinx™ 7 Series overview ds180 and Artix-7 FPGAs data sheet ds181.

Feature	XC7A200T-2FBG676I
Logic Cells	215 360
Slices	33 650
Distributed RAM (Kbit)	2 888
DSP48E1 Slices	740
Block RAM (Kbit)	13 140
Clock Management Tiles	10
Speed Grade	-2
Temperatur Range	Industrial (I): -40 to +100 °C
Bitstream Length (bit)	77 845 216

FPGA Configuration

The FPGA on EFM-03 modules can be loaded with a valid configuration file in one of several ways.

SPI Flash

The onboard Quad-SPI serial flash device Micron N25Q256A13 is the default source for configuration bitstreams at startup. At least two configuration files can be stored inside the 32 Mbyte flash device and MultiBoot is supported. To store an appropriate configuration file in flash, several ways exist.

Loading SPI Flash via USB[4]

The easiest way to write configuration data into the onboard SPI flash is to use CESYS **UDK3 Board Manager**. It uses the USB 3.0 interface of the board to write raw binary FPGA configuration bitstreams (*.bin) into the onboard SPI flash. You can find details about the UDK3 Board Manager in our user guide UG103.

Loading SPI flash via JTAG

Another way to program the SPI flash is by using the Xilinx™ Platform Cable (not included in the EFM-03 scope of delivery) and the Xilinx™ VIVADO suite. Select n25q256-3.3v-spi-x1_x2_x4 when adding a configuration memory device. To speed up FPGA configuration from serial flash, user designs can use Quad-SPI and EMCCLK option. EFM-03 comes with an onboard 90 MHz clock oscillator for highest FPGA configuration speeds from SPI flash.

Prevent SPI configuration at startup

Default configuration at startup is from the serial SPI flash device. To prevent starting from SPI flash, set Flash_Inhibit_n to a logic low level prior to enabling FPGA power supplies. After configuration using a different programming interface, Flash_Inhibit_n has to be released before access to the SPI flash is possible again.

Pin-number	Signal name	Comment
J1, pin 6	Flash_Inhibit_n	Active-low input to prevent programming of FPGA from SPI flash device at startup.

4 EFM-03 SPI programming via USB requires at least UDK3 Board Manager v1.6.

USB

EFM-03 also supports direct reprogramming of the Artix-7 FPGA via USB without altering the SPI flash content. USB configuration is available at all times, as long as FPGA power supplies are enabled. Use CESYS **UDK3 Board Manager** or the suitable function call from the CESYS UDK API to download the *.bin configuration file. Configuring the FPGA via USB3.0 is the fastest of all supported configuration modes for the EFM-03.

JTAG

The FPGA JTAG interface is routed to the expansion connector J1. All necessary pull-up resistors are already installed on the EFM-03 module. Configuration through the JTAG interface is available at all times, as long as FPGA power supplies are enabled. The JTAG programming voltage is fixed to the 3.3 Volt VCCO_0 power supply voltage, which is available at connector J1 as well.

JTAG signal name	J1 pin-number	FPGA direction	Comment
TDO	109	Out	Test data out
TMS	111	In	Test mode select
TCK	113	In	Test clock
TDI	115	In	Test data in
VCCO_0	114,116	--	3.3 Volt JTAG programming voltage

Power supply options

The EFM-03 can be operated from a single 5.0 V power source supplied at pins 1 and 3 of the expansion connector J2. onboard high-efficiency switching regulators provide all necessary power supplies: 3.3 V, 1.8 V, 1.35 V, 1.2 V, 1.0 V. A low-dropout regulator is used to derive the DDR3L termination voltage from 1.35 V. The 5.0 V USB3.0 VBUS power supply is available at pin 5 of the expansion connector J2, the 3.3V power supply is connected to pins 114 and 116 of J1. The EFM-03 is designed to support both USB power supply schemes: bus-powered and self-powered mode.

Bus-powered mode

In bus-powered mode pins 1 and 3 of the expansion connector J2 **MUST** be connected to the 5.0 V USB 3.0 VBUS power supply, which is provided at pin 5 of J2. Either install jumper J5 or plug EFM-03 module into an adequate board. Please be sure to remove jumper J5 in case an external power supply should be used. Otherwise EFM-03 or connected devices may be damaged.

According to the USB specifications, the FPGA power supplies are only switched on, when an USB connection has been established and FX-3 firmware has been downloaded successfully. PWR_ENA_EXT on pin 119 of J1 **MUST** be left open for bus-powered mode to work properly.

Self-powered mode

In self-powered mode, connect an adequate external 5.0 V power supply to J2 pins 1 and 3. Pin 5 of J2, which connects to USB3.0 VBUS power supply, should be left open. Please make sure that jumper J5 is not installed. Otherwise EFM-03 or attached devices may be damaged. NEVER connect an external power supply to J2, pin 5, as this may damage the host computers USB peripheral interface. Similar to bus-powered mode, internal logic controls the generation of FPGA power supplies and only activates these, when an USB connection has been established and FX-3 firmware has been

downloaded successfully. If FPGA power supplies shall be enabled regardless of the USB connection state, PWR_ENA_EXT on pin 119 of J1 must be driven to a logic HIGH level or connected to the external 5.0 V power supply. Then all necessary onboard power supplies are enabled as soon as the external 5.0 V power supply becomes available.

Power supply mode		J2, Pins 1,3	J2, Pin 5	J1, Pin 119
Bus-powered		Either install jumper J5 or plug EFM-03 into an adequate breakout board which connects these pins.		open
Self-powered	USB controlled	Connect to external 5.0 V power supply.	open	open
	Instant on	Connect to external 5.0 V power supply.	open	Connect to external 5.0 V power supply or drive to a logic HIGH level.

External power supply input requirements	Min.	Typ.	Max.	Units
Power supply input range at J2, Pins 1+3	4.5	5.0	5.5	V
Minimum current requirement[5]	850			mA

5 FPGA configured with EFM-03 SoC design, USB 3.0 transmission to onboard 2 Gbyte DDR3L memory at maximum speed.

Onboard peripherals

With plenty of FPGA I/O available at the expansion connectors the EFM-03 supports a vast number of applications. To help the system designer to successfully implement a Artix-7 design some crucial peripherals are installed onboard, with a VHDL reference design 'efm03_wrapper' readily available.

Quad-SPI configuration/data memory

The onboard serial flash device Micron N25Q256A13 provides 32 MByte of non-volatile storage. The flash is connected to the configuration interface of the FPGA and serves as default configuration medium. At least two FPGA configuration files can be stored in flash allowing MultiBoot operation. Remaining free storage can be used in user designs. The N25Q256A13 device supports standard Serial Peripheral Interface as well as the faster Dual-SPI and Quad-SPI modes. The flash device supports clock frequencies of up to 108 MHz, allowing data rates up to 54 MByte/s in Quad-SPI mode.

SPI Flash	FPGA Pin	Comment
DQ0	R14	Serial data IO0
DQ1	R15	Serial data IO1
C	H13[6]	Serial clock
S#	P18	Chip select
W#/DQ2	P14	Write protect[7]/Serial data IO2
HOLD#/DQ3	N14	Hold[7]/Serial data IO3

6 Connected only when FPGA configuration via USB is disabled (default mode).
7 4.7 kOhm pull-up resistor connected onboard EFM-03.

DDR3L memory

The EFM-03 module provides 2GByte of high-speed low-power DDR3L[8] memory connected to FPGA banks 34 and 35, which are supplied by an onboard 1.35 V switching power supply. The following table gives detailed information about the connections.

DDR3	FPGA Pin	FPGA Direction	Comment
DQ0	G8	Bidirectional	Bidirectional data bus bit 0
DQ1	G6	Bidirectional	Bidirectional data bus bit 1
DQ2	H6	Bidirectional	Bidirectional data bus bit 2
DQ3	H8	Bidirectional	Bidirectional data bus bit 3
DQ4	F8	Bidirectional	Bidirectional data bus bit 4
DQ5	E6	Bidirectional	Bidirectional data bus bit 5
DQ6	F7	Bidirectional	Bidirectional data bus bit 6
DQ7	D6	Bidirectional	Bidirectional data bus bit 7
DM0	H9	Output	Data mask signal for byte 0
DQS0_P, DQS0_N	H7, G7	Bidirectional	Differential data strobe signal for byte 0
DQ8	K6	Bidirectional	Bidirectional data bus bit 8
DQ9	J5	Bidirectional	Bidirectional data bus bit 9
DQ10	L8	Bidirectional	Bidirectional data bus bit 10
DQ11	F4	Bidirectional	Bidirectional data bus bit 11
DQ12	J6	Bidirectional	Bidirectional data bus bit 12
DQ13	G5	Bidirectional	Bidirectional data bus bit 13
DQ14	K8	Bidirectional	Bidirectional data bus bit 14
DQ15	G4	Bidirectional	Bidirectional data bus bit 15
DM1	K7	Output	Data mask signal for byte 1
DQS1_P, DQS1_N	J4, H4	Bidirectional	Differential data strobe signal for byte 1
DQ16	B4	Bidirectional	Bidirectional data bus bit 16
DQ17	D3	Bidirectional	Bidirectional data bus bit 17
DQ18	D5	Bidirectional	Bidirectional data bus bit 18
DQ19	F3	Bidirectional	Bidirectional data bus bit 19
DQ20	C4	Bidirectional	Bidirectional data bus bit 20
DQ21	D4	Bidirectional	Bidirectional data bus bit 21
DQ22	A4	Bidirectional	Bidirectional data bus bit 22
DQ23	E5	Bidirectional	Bidirectional data bus bit 23
DM2	C3	Output	Data mask signal for byte 2
DQS2_P, DQS2_N	B5, A5	Bidirectional	Differential data strobe signal for byte 2
DQ24	A2	Bidirectional	Bidirectional data bus bit 24

8 Type of the DDR3L devices: Alliance Inc. AS4C512M16D3L-12BCN

DDR3	FPGA Pin	FPGA Direction	Comment
DQ25	E2	Bidirectional	Bidirectional data bus bit 25
DQ26	E1	Bidirectional	Bidirectional data bus bit 26
DQ27	A3	Bidirectional	Bidirectional data bus bit 27
DQ28	D1	Bidirectional	Bidirectional data bus bit 28
DQ29	F2	Bidirectional	Bidirectional data bus bit 29
DQ30	G2	Bidirectional	Bidirectional data bus bit 30
DQ31	C2	Bidirectional	Bidirectional data bus bit 31
DM3	G1	Output	Data mask signal for byte 3
DQS3_P, DQS3_N	C1, B1	Bidirectional	Differential data strobe signal for byte 3
A0	M4	Output	Address input bit 0
A1	T4	Output	Address input bit 1
A2	U5	Output	Address input bit 2
A3	N1	Output	Address input bit 3
A4	R1	Output	Address input bit 4
A5	P1	Output	Address input bit 5
A6	M7	Output	Address input bit 6
A7	R2	Output	Address input bit 7
A8	U1	Output	Address input bit 8
A9	L4	Output	Address input bit 9
A10	L5	Output	Address input bit 10
A11	T5	Output	Address input bit 11
A12	M6	Output	Address input bit 12
A13	N7	Output	Address input bit 13
A14	K5	Output	Address input bit 14
A15	L7	Output	Address input bit 15
BA0	T2	Output	Bank address input
BA1	P6	Output	Bank address input
BA2	T3	Output	Bank address input
RAS#	H2	Output	Command input
CAS#	N4	Output	Command input
WE#	N6	Output	Command input
ODT	H1	Output	On-die termination
CK_P, CK_N	N3, N2	Output	Differential memory clock
CKE	J1	Output	Clock enable
CS#	P4	Output	Chip select
RESET#	N8	Output	
ZQ0, ZQ1	--	--	Connected to GND via 240 Ohm resistor for ODT calibration

USB 2.0-UART

For in- design debug purposes of your FPGA design you can use the serial UART interface provided onboard by one FTDI FT230X device. The USB to BASIC UART interface is available at the USB 2.0 Mini-B connector. Device connections are summarized in the following table. For more details about the FTDI FT230X please refer to the datasheet available at www.ftdichip.com.

USB-to-UART Signal Name	FPGA Pin	FPGA Direction	Comment
USBDM, USBDP	--	--	Differential USB data signal pair.
RxD	T7	Out	Receiving Asynchronous Data Input.
TxD	R6	In	Transmit Asynchronous Data Output.
RTS#	T8	In	Request to Send Control Output / Handshake Signal.
CTS#	R7	Out	Clear To Send Control Input / Handshake Signal.
CBUS0	--	--	Not connected.
CBUS1	--	--	RXLED#. Pulses low when receiving data via USB. Lights up led D10.
CBUS2	--	--	TXLED#. Pulses low when transmitting data via USB. Lights up led D9.
CBUS3	--	--	SLEEP#. Goes low during USB suspend mode. Availabe at test pad TP3.
RESET#	--	--	FTDI reset input (active low). Connected to Micro-B VBUS2 power supply through resistor network.

Status leds

Three leds give basic information about power and configuration status of the EFM-03 module.

Led	Color	Function	Comment
D1	Green	DONE	Lights up, when FPGA is configured.
D2	Red	ERROR	Lights up, when some error occurs during FPGA initialization.
D14	Green	OK	Lights up, when FPGA initialization was successful.

LED D1 connects to the FPGA DONE output signal. Whenever a valid configuration file is stored within FPGA SRAM this led will light up green. Leds D2 and D14 are connected to the FPGA INIT_B pin, signaling information about FPGA initialization status.

User led

In addtion to the three status leds mentioned above, EFM-03 provides one user accessible led. D7 is controllable through FPGA pin N23. Use it for additional user specific status information. A HIGH level output will turn the blue led on.

Led	Color	FPGA Pin	Comment
D7	Blue	N23	Set HIGH to light up led.

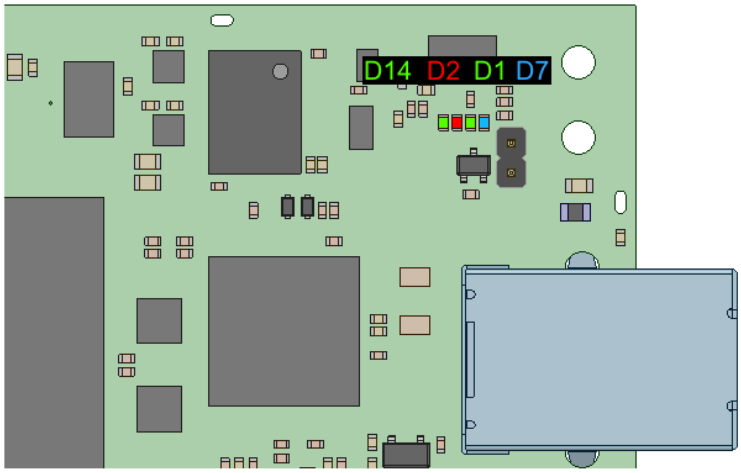


Figure 2: EFM-03: User and status leds

Onboard clocks

EFM-03 offers two onboard clock oscillators. One, a high performance 200 MHz LVDS clock oscillator, is used to provide a high stability system clock. The other, a 90 MHz low power CMOS oscillator, is connected to the EMCCLK input pin of the Xilinx™ Artix-7 device.

High-stability LVDS system clock oscillator

EFM-03 provides a high-stability 200 MHz differential system clock on FPGA balls R3 and P3. FPGA internal PLL / DCM can be used to generate a multitude of clock signals. See the following table for some specifications.

Parameter	Value
Frequency	200 MHz
Frequency stability	+/-50 ppm
RMS phase jitter (typ.)	0.7 ps
RMS period jitter (max.)	3.5 ps
Output rise/fall time (typ.)	260 ps
Differential output voltage (typ.)	350 mV
FPGA balls for SYSCLK_P, SYSCLK_N	R3, P3

Low power CMOS oscillator

To enable the highest possible configuration speeds from SPI flash with predictable configuration times, EFM-03 provides a 90 MHz low power CMOS oscillator on the EMCCLK input pin. For further information about Master SPI configuration mode and the usage of the EMCCLK clock input with your design, please consult the Xilinx™ 7 Series FPGAs Configuration guide ug470.

Parameter	Value
Frequency	90 MHz
Frequency stability	+/-50 ppm
RMS phase jitter (typ.)	1.3 ps
RMS period jitter (max.)	3 ps
Output rise/fall time (typ.)	1 ns
FPGA ball for EMCCLK	P16

SuperSpeed USB 3.0

EFM-03 provides a SuperSpeed USB 3.0[9] interface using the versatile controller CYUSB3014-BZ from Cypress Semiconductor. To keep up with the enormously high USB 3.0 data rates, a 32 bit Slave FIFO interface running at 100 MHz is used for communication between FPGA and the EZ-USB FX3. See CESYS UG104 UDK3-Performance-Monitor for benchmarks and CESYS UG121 axi-fx3-interface for a close description of a slave-fifo interface reference design.

I²C EEPROM

EFM-03 includes the 1 Mbit Atmel™ AT24CM01-XHM I²C EEPROM to store VID/PID data for the USB enumeration process.

In case you decide to develop your own FX3 firmware and store it inside non-volatile memory rather than downloading it via USB, it may be required to increase the available memory due to the size of FX3 firmware images. To increase available storage EZ-USB FX3 supports multiple EEPROM devices of the same size and type sharing the I²C bus. The firmware image then should be stored across the EEPROMs as a contiguous image as in a single I²C device. On more information about EZ-FX3 boot options using the I²C interface please consult the application note AN76405 from Cypress™. EZ-USB FX3's I²C interface is available at the expansion connector J2.

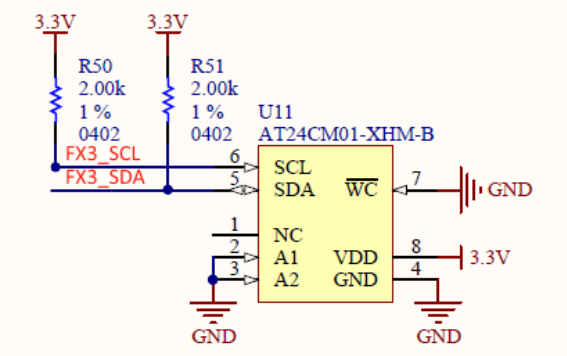


Figure 3: EZ-USB FX3 I²C EEPROM

FX3	Exp.	FX3 Direction	Comment
FX3_SDA	J2, 18	Bidirectional (Open drain)	I²C interface data line
FX3_SCL	J2, 20	Output (Open drain)	I²C interface clock signal
VIO5	J2, 15		I²C power supply output
GND	J2, GND		GND power terminal

9 Please note, that EZ-USB FX3 boot loader works in USB 2.0 mode. With EFM-03 the default boot mode is via USB, therefore USB 2.0 D+/D- lines are still required, even if user applications would only use SuperSpeed USB 3.0 mode.

Slave FIFO interface

The synchronous Slave FIFO interface uses a 32 bit parallel data bus and several status/control I/O to perform data read/write accesses to EZ-USB FX3's internal FIFO buffers. Register accesses are not done using the Slave FIFO interface. See the following table for a list of connections between FPGA and EZ-USB FX3 used for the host interface. For more information about how you can use EFM-03's USB 3.0 interface please consult CESYS ug101-udk3-api-specification and the EFM-03-SoC reference design.

FX3	FPGA Pin	FPGA Direction	Comment
PCLK	N21, M21	Output/Input	Slave FIFO interface clock
DQ0	T24	Bidirectional	Bidirectional data bus bit 0
DQ1	L23	Bidirectional	Bidirectional data bus bit 1
DQ2	L22	Bidirectional	Bidirectional data bus bit 2
DQ3	L24	Bidirectional	Bidirectional data bus bit 3
DQ4	N16	Bidirectional	Bidirectional data bus bit 4
DQ5	N17	Bidirectional	Bidirectional data bus bit 5
DQ6	R16	Bidirectional	Bidirectional data bus bit 6
DQ7	R17	Bidirectional	Bidirectional data bus bit 7
DQ8	N18	Bidirectional	Bidirectional data bus bit 8
DQ9	K25	Bidirectional	Bidirectional data bus bit 9
DQ10	K26	Bidirectional	Bidirectional data bus bit 10
DQ11	M20	Bidirectional	Bidirectional data bus bit 11
DQ12	L20	Bidirectional	Bidirectional data bus bit 12
DQ13	L25	Bidirectional	Bidirectional data bus bit 13
DQ14	M24	Bidirectional	Bidirectional data bus bit 14
DQ15	M25	Bidirectional	Bidirectional data bus bit 15
DQ16	R23	Bidirectional	Bidirectional data bus bit 16
DQ17	T23	Bidirectional	Bidirectional data bus bit 17
DQ18	R22	Bidirectional	Bidirectional data bus bit 18
DQ19	T22	Bidirectional	Bidirectional data bus bit 19
DQ20	P26	Bidirectional	Bidirectional data bus bit 20
DQ21	R26	Bidirectional	Bidirectional data bus bit 21
DQ22	T25	Bidirectional	Bidirectional data bus bit 22
DQ23	M26	Bidirectional	Bidirectional data bus bit 23
DQ24	N26	Bidirectional	Bidirectional data bus bit 24
DQ25	P25	Bidirectional	Bidirectional data bus bit 25
DQ26	R25	Bidirectional	Bidirectional data bus bit 26
DQ27	R21	Bidirectional	Bidirectional data bus bit 27

FX3	FPGA Pin	FPGA Direction	Comment
DQ28	R20	Bidirectional	Bidirectional data bus bit 28
DQ29	P24	Bidirectional	Bidirectional data bus bit 29
DQ30	P23	Bidirectional	Bidirectional data bus bit 30
DQ31	N19	Bidirectional	Bidirectional data bus bit 31
SLCS#	M22	Output	Chip select for Slave FIFO interface
SLWR#	M19	Output	Write strobe for Slave FIFO interface
SLRD#	K16	Output	Read strobe for Slave FIFO interface
SLOE#	K17	Output	Output enable
PKTEND	L19	Output	Short packet signal
FLAGA	P21	Input	Flag output from FX3
FLAGB	N24	Input	Flag output from FX3
GPIO23 / CTL[6]	J16	Input	EZ-FX3 GPIO or control output
GPIO25 / CTL[8]	J15	Input	EZ-FX3 GPIO or control output[10]
GPIO26 / CTL[9]	R18	Input	EZ-FX3 GPIO or control output
GPIO27 / CTL[10]	J14	Input	EZ-FX3 GPIO or control output
CTL[15]	K18	Input	EZ-FX3 control output (16Bit modes only)
A0	P20	Output	Address input of Slave FIFO interface
A1	N22	Output	Address input of Slave FIFO interface
GPIO54	K15	Input	FPGA RESET[11]

10 Connected to FPGA CCLK during configuration via USB.
11 Software settable active-high reset signal. Used during configuration via USB for synchronization purposes. Pull-up resistor connected onboard EFM-03.

FX3 additional connections

For configuration purposes some additional connections between Xilinx™ FPGA and Cypress™ EZ-USB FX3 are necessary. The following chart gives some information about these and where to find them on the expansion connector J1.
Additionally GPIO55 and GPIO56 of Cypress™ EZ-USB FX3 are routed to the expansion connector J2. However with EFM-03 default firmware those GPIO signals are not implemented. Please refer to the EZ-USB FX3's data sheet on Cypress™ website for more information about usability of GPIO signals.

FX3	Expansion Connector	FPGA Pin	FPGA Direction	Comment
GPIO45	--	--	--	USB_CONFIGn[12]
GPIO50	--	P19	Input	FPGA_CSI_B
GPIO51	J1, Pin10	W10	Output[13]	Done
GPIO52	J1, Pin4	V11	Input/Output[13]	Init_B
GPIO53	J1, Pin8	AE16	Input	Program_B
GPIO54	J2, Pin24	K15	Input	FPGA RESET[14]
GPIO55	J2, Pin19	--	--	FX3 GPIO
GPIO56	J2, Pin21	--	--	FX3 GPIO
GPIO57	--	--	--	FPGA power enable[15]

12 A logic HIGH level enables FGPA configuration via USB. SPI flash clock MUST be set to tri-state mode prior to enabling USB configuration mode, for example by pulling Program_B low.
13 Open drain.
14 Software settable active-high reset signal. Used during configuration via USB for synchronization purposes. Pull-up resistor connected onboard EFM-03.
15 A logic HIGH level enables FPGA power supplies. See EFM-03 power supply options for more details.

Digital IO expansion connectors

Two 0,80mm 120-pin Q Strip high-speed ground plane expansion connectors (Samtec™: QSE-060-01-L-D-A) on the bottom-side of the EFM-03 offer access to up to 191 FPGA I/O, two FX3 GPIO, FX3 I²C interface, FX3 and FPGA JTAG signals, some configuration I/O and selected power rails. Optionally USB signals are available. As default all I/O are configured for 3.3 V LVTTL signaling levels. Optionally VCCO power supplies for selected banks of the Artix-7 FPGA can be accessed independently. Then an adequate power supply has to be connected to the corresponding expansion pins to set the required signaling level. Additionally one 0.80 mm 40-pin Q Strip high-speed ground plane expansion connector (Samtec™: QSE-020-01-L-D-A) offers access to all receiver, transmitter and reference clock pairs of the Artix-7 FPGA GTP blocks MGT213 and MGT216.
Samtec™ offers mating connectors in several variations resulting in different total mating heights. See the following table for some information. Please refer to the Samtec™ website for details.

Samtec™ part number	Mated height
QTE-060-01-L-D	5.00 mm
QTE-060-02-L-D	8.00 mm
QTE-060-03-L-D	11.00 mm
QTE-060-04-L-D	16.00 mm
QTE-060-05-L-D	19.00 mm
QTE-060-07-L-D	25.00 mm

Pinout expansion connector J1

J1	FPGA Ball	Pin Group[16]	Description	J1	FPGA Ball	Pin Group	Description
1	F25	PG2, IO9N	IO_L23N_T3_15	**2**	--	--	FX3 32kHz clock in
3	G25	PG2, IO9P	IO_L23P_T3_15	**4**		--	FPGA Init_B
5	G26	PG2, IO8N	IO_L22N_T3_15	**6**	--	--	Flash_Inhibit_N[17]
7	H26	PG2, IO8P	IO_L22P_T3_15	**8**		--	FPGA Program_B
9	H24	PG2, IO2N	IO_L16N_T2_15	**10**		--	FPGA Done
11	J24	PG2, IO2P	IO_L16P_T2_15	**12**	J25	PG2, IO20	IO_L24P_T3_15
13	**--**	**--**	**1.8V power output[18]**	**14**	L15	PG2, IO1N	IO_L5N_T0_AD9N_15
15	**--**	**--**	**1.8V power output[18]**	**16**	M15	PG2, IO1P	IO_L5P_T0_AD9P_15
17	Y26	PG0, IO4N	IO_L4N_T0_13	**18**	L18	PG2, IO13N	IO_L8N_T1_AD10N_15
19	W25	PG0, IO4P	IO_L4P_T0_13	**20**	L17	PG2, IO13P	IO_L8P_T1_AD10P_15
21	Y23	PG0, IO1N	IO_L11N_T1_SRCC_13	**22**	M17	PG2, IO10N	IO_L6N_T0_15
23	Y22	PG0, IO1P	IO_L11P_T1_SRCC_13	**24**	M16	PG2, IO10P	IO_L6P_T0_15
25	V24	PG0, IO7P	IO_L6P_T0_13	**26**	L14	PG2, IO0N	IO_L4N_T0_15
27	W24	PG0, IO7N	IO_L6N_T0_VREF_13	**28**	M14	PG2, IO0P	IO_L4P_T0_15
29	AA23	PG0, IO9N	IO_L8N_T1_13	**30**	V23	PG0, IO11P	IO_L10P_T1_13
31	AA22	PG0, IO9P	IO_L8P_T1_13	**32**	W23	PG0, IO11N	IO_L10N_T1_13
33	AB25	PG0, IO8N	IO_L7N_T1_13	**34**	Y25	PG0, IO6P	IO_L5P_T0_13
35	AA24	PG0, IO8P	IO_L7P_T1_13	**36**	AA25	PG0, IO6N	IO_L5N_T0_13
37	U22	PG0, IO5P	IO_L12P_T1_MRCC_13	**38**	W21	PG0, IO23P	IO_L14P_T2_MRCC_13
39	V22	PG0, IO5N	IO_L12N_T1_MRCC_13	**40**	Y21	PG0, IO23N	IO_L14N_T2_MRCC_13

16 FPGA IO within the same pin group (PG0, PG1, PG2) are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.

17 Flash_Inhibit_N: Default FPGA configuration at startup is from SPI flash. To prevent SPI configuration, drive this pin to a logic LOW level, prior to enabling FPGA power supplies.

18 Onboard 1A switching power supply output. Also supplies FPGA auxiliary voltage VCCAUX.

J1	FPGA Ball	Pin Group[19]	Description	J1	FPGA Ball	Pin Group	Description
41	AA20	PG0, IO27P	IO_L12P_T1_MRCC_12	**42**	V26	PG0, IO2P	IO_L2P_T0_13
43	AB20	PG0, IO27N	IO_L12N_T1_MRCC_12	**44**	W26	PG0, IO2N	IO_L2N_T0_13
45	AD21	PG0, IO32P	IO_L7P_T1_12	**46**	U26	PG0, IO0N	IO_L1N_T0_13
47	AE21	PG0, IO32N	IO_L7N_T1_12	**48**	U25	PG0, IO0P	IO_L1P_T0_13
49	AE22	PG0, IO30P	IO_L9P_T1_DQS_12	**50**	AC26	PG0, IO3N	IO_L3N_T0_DQS_13
51	AF22	PG0, IO30N	IO_L9N_T1_DQS_12	**52**	AB26	PG0, IO3P	IO_L3P_T0_DQS_13
53	AD20	PG0, IO29P	IO_L10P_T1_12	**54**	AB24	PG0, IO10P	IO_L9P_T1_DQS_13
55	AE20	PG0, IO29N	IO_L10N_T1_12	**56**	AC24	PG0, IO10N	IO_L9N_T1_DQS_13
57	AF20	PG0, IO31N	IO_L8N_T1_12	**58**	AB21	PG0, IO28P	IO_L11P_T1_SRCC_12
59	AF19	PG0, IO31P	IO_L8P_T1_12	**60**	AC21	PG0, IO28N	IO_L11N_T1_SRCC_12
61	AE18	PG0, IO24P	IO_L16P_T2_12	**62**	Y20	PG0, IO14N	IO_L16N_T2_13
63	AF18	PG0, IO24N	IO_L16N_T2_12	**64**	W20	PG0, IO14P	IO_L16P_T2_13
65	AB19	PG0, IO33N	IO_L13N_T2_MRCC_12	**66**	J18	PG2, IO15P	IO_L10P_T1_AD11P_15
67	AA19	PG0, IO33P	IO_L13P_T2_MRCC_12	**68**	H18	PG2, IO15N	IO_L10N_T1_AD11N_15
69	T20	PG0, IO13P	IO_L15P_T2_DQS_13	**70**	AD19	PG0, IO26N	IO_L14N_T2_SRCC_12
71	U20	PG0, IO13N	IO_L15N_T2_DQS_13	**72**	AC19	PG0, IO26P	IO_L14P_T2_SRCC_12
73	T19	PG0, IO15P	IO_L17P_T2_13	**74**	AD18	PG0, IO25N	IO_L15N_T2_DQS_12
75	U19	PG0, IO15N	IO_L17N_T2_13	**76**	AC18	PG0, IO25P	IO_L15P_T2_DQS_12
77	W19	PG0, IO16N	IO_L18N_T2_13	**78**	T18	PG0, IO19N	IO_L21N_T3_DQS_13
79	V19	PG0, IO16P	IO_L18P_T2_13	**80**	T17	PG0, IO19P	IO_L21P_T3_DQS_13

19 FPGA IO within the same pin group (PG0, PG1, PG2) are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.

J1	FPGA Ball	Pin Group[20]	Description	J1	FPGA Ball	Pin Group	Description
81	W18	PG0, IO17N	IO_L19N_T3_VREF_13	**82**	**--**	**PG0**	**Optional power supply input for FPGA pin group PG0[21]**
83	V18	PG0, IO17P	IO_L19P_T3_13	**84**	**--**	**PG0**	**Optional power supply input for FPGA pin group PG0[21]**
85	AE5	PG1, IO26N	IO_L15N_T2_DQS_33	**86**	V14	PG0, IO21N	IO_L23N_T3_13
87	AD5	PG1, IO26P	IO_L15P_T2_DQS_33	**88**	U14	PG0, IO21P	IO_L23P_T3_13
89	V17	PG0, IO22N	IO_L24N_T3_13	**90**	T15	PG0, IO18N	IO_L20N_T3_13
91	V16	PG0, IO22P	IO_L24P_T3_13	**92**	T14	PG0, IO18P	IO_L20P_T3_13
93	AD4	PG1, IO38N	IO_L18N_T2_33	**94**	U21	PG0, IO12P	IO_L13P_T2_MRCC_13
95	AC4	PG1, IO38P	IO_L18P_T2_33	**96**	V21	PG0, IO12N	IO_L13N_T2_MRCC_13
97	AC6	PG1, IO34N	IO_L24N_T3_33	**98**	AC3	PG1, IO27P	IO_L14P_T2_SRCC_33
99	AB6	PG1, IO34P	IO_L24P_T3_33	**100**	AD3	PG1, IO27N	IO_L14N_T2_SRCC_33
101	U16	PG0, IO20N	IO_L22N_T3_13	**102**	AF3	PG1, IO25N	IO_L16N_T2_33
103	U15	PG0, IO20P	IO_L22P_T3_13	**104**	AE3	PG1, IO25P	IO_L16P_T2_33
105	AF5	PG1, IO24P	IO_L17P_T2_33	**106**	AB2	PG1, IO30P	IO_L11P_T1_SRCC_33
107	AF4	PG1, IO24N	IO_L17N_T2_33	**108**	AC2	PG1, IO30N	IO_L11N_T1_SRCC_33
109		--	FPGA TDO	**110**	AE1	PG1, IO32N	IO_L9N_T1_DQS_33
111		--	FPGA TMS	**112**	AD1	PG1, IO32P	IO_L9P_T1_DQS_33
113		--	FPGA TCK	**114**	**--**	**PG2**	**3.3V power output[22]**
115		--	FPGA TDI	**116**	**--**	**PG2**	**3.3V power output[22]**
117	--	--	Not connected	**118**	AE2	PG1, IO31P	IO_L10P_T1_33
119	--	--	FPGA power enable input[23]	**120**	AF2	PG1, IO31N	IO_L10N_T1_33

20 FPGA IO within the same pin group (PG0, PG1, PG2) are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.

21 With the default assembly option pin group PG0 is supplied by the onboard 3.3 Volt power supply through a 0 Ohm series resistor. Optionally PG0 can be powered externally to support signaling levels other than the default 3.3 Volt LVTTL. For details about signal levels supported by Xilinx™ 7 Series FPGAs, please refer to guide ug471. **CAUTION**: Resistor R104 **MUST** not be set in this case.

22 Onboard 3A switching power supply output. Also supplies FPGA pin group PG2, JTAG and FX3 VIO.

23 Internal logic controls FPGA power supplies. If FPGA power supplies need to be enabled regardless of USB connection status, drive this pin to a logic HIGH level (LVTTL 3.3V) or connect to VBUS_IO.

Pinout expansion connector J2

J2	FPGA Ball	Pin Group[24]	Description	J2	FPGA Ball	Pin Group	Description
1	**--**	**--**	**5.0 V input (VBUS_IO)[25]**	**2**	--	--	USB 2.0 D-[27]
3	**--**	**--**	**5.0 V input (VBUS_IO)[25]**	**4**	--	--	USB 2.0 D+[27]
5	**--**	**--**	**5.0 V output (USB VBUS1)[26]**	**6**	--	--	USB OTG ID[27]
7	--	--	USB 3.0 TX-[27]	**8**	--	--	FX3 TRSTn
9	--	--	USB 3.0 TX+[27]	**10**	--	--	FX3 TDO
11	--	--	USB 3.0 RX+[27]	**12**	--	--	FX3 TMS
13	--	--	USB 3.0 RX-[27]	**14**	--	--	FX3 TDI
15	--	--	FX3 I²C power supply output.[28]	**16**	--	--	FX3 RESET# input[29]
17	--	--	FX3 TCK	**18**	--	--	FX3 SDA: I²C data IO
19	--	--	FX3 GPIO55	**20**	--	--	FX3 SCL: I²C clock output
21	--	--	FX3 GPIO56	**22**	--	--	Not connected
23	--	--	Not connected	**24**	K15	PG2	FPGA RESET[30]
25	E26	PG2, IO7P	IO_L21P_T3_DQS_15	**26**	K20	PG2, IO14P	IO_L09P_T1_DQS_AD3P_15
27	D26	PG2, IO7N	IO_L21N_T3_DQS_15	**28**	J20	PG2, IO14N	IO_L09N_T1_DQS_AD3N_15
29	E25	PG2, IO6P	IO_L20P_T3_15	**30**	F23	PG2, IO3P	IO_L17P_T2_15
31	D25	PG2, IO6N	IO_L20N_T3_15	**32**	E23	PG2, IO3N	IO_L17N_T2_15
33	K23	PG2, IO4N	IO_L18N_T2_15	**34**	H22	PG2, IO17N	IO_L13N_T2_MRCC_15
35	K22	PG2, IO4P	IO_L18P_T2_15	**36**	H21	PG2, IO17P	IO_L13P_T2_MRCC_15
37	J23	PG2, IO18P	IO_L14P_T2_SRCC_15	**38**	J19	PG2, IO11P	IO_L7P_T1_AD2P_15
39	H23	PG2, IO18N	IO_L14N_T2_SRCC_15	**40**	H19	PG2, IO11N	IO_L7N_T1_AD2N_15

24 FPGA IO within the same pin group (PG0, PG1, PG2) are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.
25 EFM-03 power supply input. Either connect USB VBUS1 or an adequate 5.0 Volt power supply.
26 Directly connected to USB 3.0 VBUS power supply through a ferrite bead.
27 Reserved. Requires special assembly option. See ordering information for more details.
28 Onboard 3 A switching power supply output. Also supplies FPGA pin group PG2, JTAG and FX3 VIO.
29 Active-low reset signal for FX3. Onboard EFM-03, no driving source is present. Custom boards have to connect a pull-up resistor (typical 10k Ohm) between pin 16 and pin 15 (FX3 power supply output).
30 Software settable active-high reset signal. Used during configuration via USB for synchronization purposes. Pull-up resistor connected onboard EFM-03.

J2	FPGA Ball	Pin Group[31]	Description	J2	FPGA Ball	Pin Group	Description
41	K21	PG2, IO12P	IO_L12P_T1_MRCC_15	**42**	C26	PG1, IO21P	IO_L22P_T3_16
43	J21	PG2, IO12N	IO_L12N_T1_MRCC_15	**44**	B26	PG1, IO21N	IO_L22N_T3_16
45	G24	PG2, IO5P	IO_L19P_T3_15	**46**	B25	PG1, IO19P	IO_L20P_T3_16
47	F24	PG2, IO5N	IO_L19N_T3_15	**48**	A25	PG1, IO19N	IO_L20N_T3_16
49	D24	PG1, IO23N	IO_L24N_T3_16	**50**	A24	PG1, IO20N	IO_L21N_T3_DQS_16
51	D23	PG1, IO23P	IO_L24P_T3_16	**52**	A23	PG1, IO20P	IO_L21P_T3_DQS_16
53	C23	PG1, IO16N	IO_L19N_T3_VREF_16	**54**	B22	PG1, IO13P	IO_L17P_T2_16
55	C22	PG1, IO16P	IO_L19P_T3_16	**56**	A22	PG1, IO13N	IO_L17N_T2_16
57	G22	PG2, IO19P	IO_L15P_T2_DQS_15	**58**	C21	PG1, IO12P	IO_L16P_T2_16
59	F22	PG2, IO19N	IO_L15N_T2_DQS_15	**60**	B21	PG1, IO12N	IO_L16N_T2_16
61	--	--	**1.2V power output[32]**	**62**	G21	PG2, IO16N	IO_L11N_T1_SRCC_15
63	--	--	**1.2V power output[32]**	**64**	G20	PG2, IO16P	IO_L11P_T1_SRCC_15
65	D21	PG1, IO15N	IO_L18N_T2_16	**66**	D20	PG1, IO10N	IO_L14N_T1_SRCC_16
67	E21	PG1, IO15P	IO_L18P_T2_16	**68**	E20	PG1, IO10P	IO_L14P_T1_SRCC_16
69	A18	PG1, IO8N	IO_L9N_T1_DQS_16	**70**	B24	PG1, IO22N	IO_L23N_T3_16
71	A17	PG1, IO8P	IO_L9P_T1_DQS_16	**72**	C24	PG1, IO22P	IO_L23P_T3_16
73	G16	PG1, IO5N	IO_L6N_T0_VREF_16	**74**	F20	PG1, IO4N	IO_L5N_T0_16
75	H16	PG1, IO5P	IO_L6P_T0_16	**76**	G19	PG1, IO4P	IO_L5P_T0_16
77	C18	PG1, IO17N	IO_L12N_T1_MRCC_16	**78**	C19	PG1, IO18N	IO_L13N_T2_MRCC_16
79	D18	PG1, IO17P	IO_L12P_T1_MRCC_16	**80**	D19	PG1, IO18P	IO_L13P_T2_MRCC_16

31 FPGA IO within the same pin group (PG0, PG1, PG2) are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.

32 Onboard 3 A switching power supply output. Also supplies FPGA GTP blocks and FX3 core.

J2	FPGA Ball	Pin Group[33]	Description	J2	FPGA Ball	Pin Group	Description
81	P16	PG2	Optional EMCCLK output[34]	**82**	F19	PG1, IO2N	IO_L3N_T0_DQS_16
83	G14	--	FPGA VCCBATT input	**84**	F18	PG1, IO2P	IO_L3P_T0_DQS_16
85	J26	PG2	IO_L24N_T3_15[35]	**86**	G17	PG1, IO1P	IO_L2P_T0_16
87	--	--	Not connected	**88**	F17	PG1, IO1N	IO_L2N_T0_16
89	U7	PG1, IO35P	IO_L6P_T0_33	**90**	C17	PG1, IO6P	IO_L7P_T1_16
91	V7	PG1, IO35N	IO_L6N_T0_VREF_33	**92**	B17	PG1, IO6N	IO_L7N_T1_16
93	AA8	PG1, IO40N	IO_L23N_T3_33	**94**	D16	PG1, IO7N	IO_L8N_T1_16
95	Y8	PG1, IO40P	IO_L23P_T3_33	**96**	E16	PG1, IO7P	IO_L8P_T1_16
97	E17	PG1, IO14P	IO_L11P_T1_SRCC_16	**98**	A20	PG1, IO11N	IO_L15N_T2_DQS_16
99	E18	PG1, IO14N	IO_L11N_T1_SRCC_16	**100**	B20	PG1, IO11P	IO_L15P_T2_DQS_16
101	AA4	PG1, IO28P	IO_L13P_T2_MRCC_33	**102**	F15	PG1, IO3N	IO_L4N_T0_16
103	AB4	PG1, IO28N	IO_L13N_T2_MRCC_33	**104**	G15	PG1, IO3P	IO_L4P_T0_16
105	V6	PG1, IO37P	IO_L4P_T0_33	**106**	AA3	PG1, IO29P	IO_L12P_T1_MRCC_33
107	W6	PG1, IO37N	IO_L4N_T0_33	**108**	AA2	PG1, IO29N	IO_L12N_T1_MRCC_33
109	Y7	PG1, IO33P	IO_L19P_T3_33	**110**	H15	PG1, IO0N	IO_L1N_T0_16
111	AA7	PG1, IO33N	IO_L19N_T3_VREF_33	**112**	H14	PG1, IO0P	IO_L1P_T0_16
113	V3	PG1, IO39P	IO_L3P_T0_DQS_33	**114**	A19	PG1, IO9N	IO_L10N_T1_16
115	V2	PG1, IO39N	IO_L3N_T0_DQS_33	**116**	B19	PG1, IO9P	IO_L10P_T1_16
117	Y3	PG1, IO36N	IO_L5N_T0_33	**118**	**--**	**PG1**	**Optional power supply input for FPGA pin group PG1[36]**
119	W3	PG1, IO36P	IO_L5P_T0_33	**120**	**--**	**PG1**	**Optional power supply input for FPGA pin group PG1[36]**

33 FPGA IO within the same pin group (PG0, PG1, PG2) are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.

34 As default this pin is not connected. When series resistor R28 on EFM-03 is set, this pin connects to the 90 MHz clock oscillator used for EMCCLK generation. On EFM-02/B this pin was connected to the optional clock oscillator which could be used as USERCCLK input.

35 On EFM-02/B the 100 MHz system clock was available at this pin. To provide compatibility to older hardware, user designs might be required to provide an equivalent clock output here.

36 With the default assembly option pin group PG1 is supplied by the onboard 3.3 Volt power supply through a 0 Ohm series resistor. Optionally PG1 can be powered externally to support signaling levels other than the default 3.3 Volt LVTTL. For details about signal levels supported by Xilinx™ 7 Series FPGAs, please refer to guide ug471. **CAUTION**: Resistor R105 **MUST** not be set in this case.

Non-default signal levels on PG0 and PG1

To support signal levels[37] other than the default 3.3 V LVTTL, VCCO power supplies for the EFM-03 pin groups PG0 and PG1 optionally can be sourced externally. Both pin group power supplies are routed independently from all other power supplies onboard the EFM-03 and only connected to the 3.3 V power rail by series resistors R104 and R105 respectively. Once one or both resistors are removed, VCCO power for the corresponding pin group has to be supplied on the respective input pins on the IO expansion connectors J1 and J2.

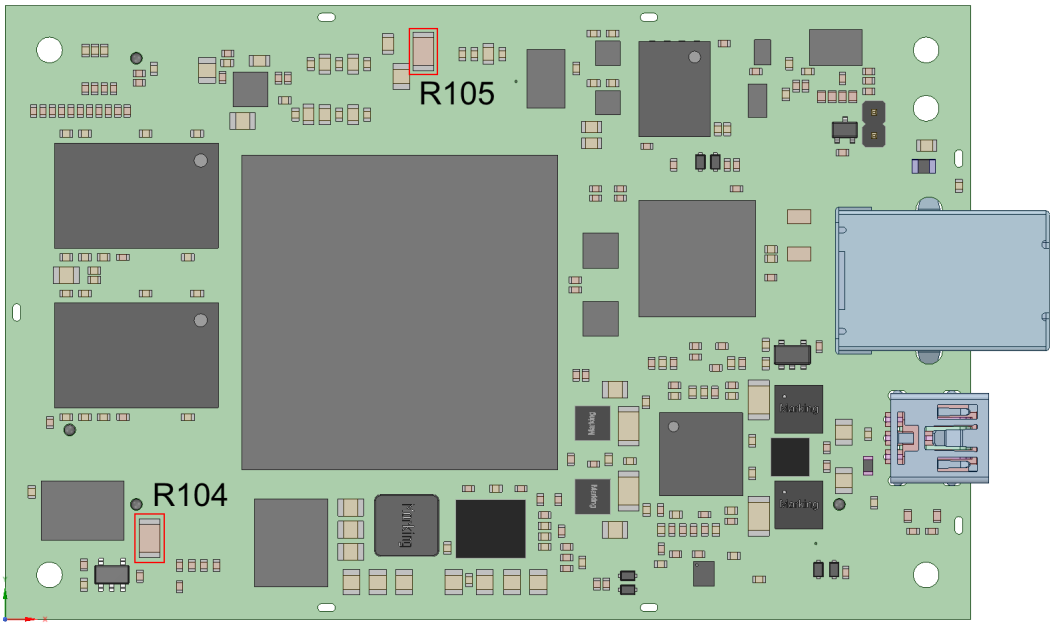


Figure 4: Series resistors for VCCO of PG0 / PG1 on EFM-03.

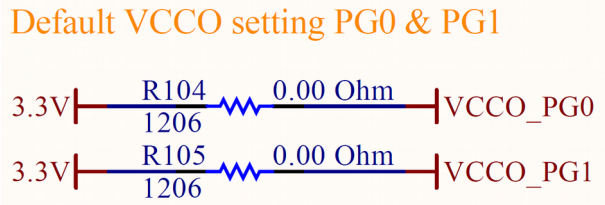


Figure 5: EFM-03: Series resistors for VCCO_PGO and VCCO_PG1

37 For details about signal levels supported by Xilinx™ 7 Series FPGAs, please refer to guide ug471.

GTP Quad expansion connector

Additionally to the two 120-pin IO connectors, EFM-03 provides one 0.80 mm 40-pin Q Strip high-speed ground plane expansion connector (Samtec™: QSE-020-01-L-D-A). Connector J6 offers access to all differential receiver, transmitter and reference clock pairs of the Artix-7 FPGA GTP blocks MGT213 and MGT216. For more details about GTP Quad Transceivers in Series 7 FPGAs please refer to Xilinx™ UG482.
Samtec™ offers mating connectors in several variations resulting in different total mating heights. Please refer to the Samtec™ website for details.

Samtec™ part number	Mated height
QTE-020-01-L-D	5.00 mm
QTE-020-02-L-D	8.00 mm
QTE-020-03-L-D	11.00 mm
QTE-020-04-L-D	16.00 mm
QTE-020-05-L-D	19.00 mm
QTE-020-07-L-D	25.00 mm

J6	FPGA Ball	Description	J6	FPGA Ball	Description
1	A9	MGT216 - MGTPTXN2	**2**	D14	MGT216 - MGTPRXP1
3	B9	MGT216 - MGTPTXP2	**4**	C14	MGT216 - MGTPRXN1
5	C10	MGT216 - MGTPTXN3	**6**	B13	MGT216 - MGTPRXP2
7	D10	MGT216 - MGTPTXP3	**8**	A13	MGT216 - MGTPRXN2
9	A7	MGT216 - MGTPTXN0	**10**	B11	MGT216 - MGTPRXP0
11	B7	MGT216 - MGTPTXP0	**12**	A11	MGT216 - MGTPRXN0
13	C8	MGT216 - MGTPTXN1	**14**	D12	MGT216 - MGTPRXP3
15	D8	MGT216 - MGTPTXP1	**16**	C12	MGT216 - MGTPRXN3
17	E13	MGT216 - MGTREFCLK1N	**18**	F11	MGT216 - MGTREFCLK0P
19	F13	MGT216 - MGTREFCLK1P	**20**	E11	MGT216 - MGTREFCLK0N
21	AA13	MGT213 - MGTREFCLK0P	**22**	AB11	MGT213 - MGTREFCLK1N
23	AB13	MGT213 - MGTREFCLK0N	**24**	AA11	MGT213 - MGTREFCLK1P
25	AC8	MGT213 - MGTPTXP2	**26**	AF11	MGT213 - MGTPRXN3
27	AD8	MGT213 - MGTPTXN2	**28**	AE11	MGT213 - MGTPRXP3
29	AE7	MGT213 - MGTPTXP3	**30**	AF13	MGT213 - MGTPRXN1
31	AF7	MGT213 - MGTPTXN3	**32**	AE13	MGT213 - MGTPRXP1
33	AE9	MGT213 - MGTPTXP1	**34**	AD12	MGT213 - MGTPRXN0
35	AF9	MGT213 - MGTPTXN1	**36**	AC12	MGT213 - MGTPRXP0
37	AC10	MGT213 - MGTPTXP0	**38**	AF13	MGT213 - MGTPRXN2
39	AD10	MGT213 - MGTPTXN0	**40**	AC14	MGT213 - MGTPRXP2

Evaluation

EFM-03 on EFM-03 Breakout Board

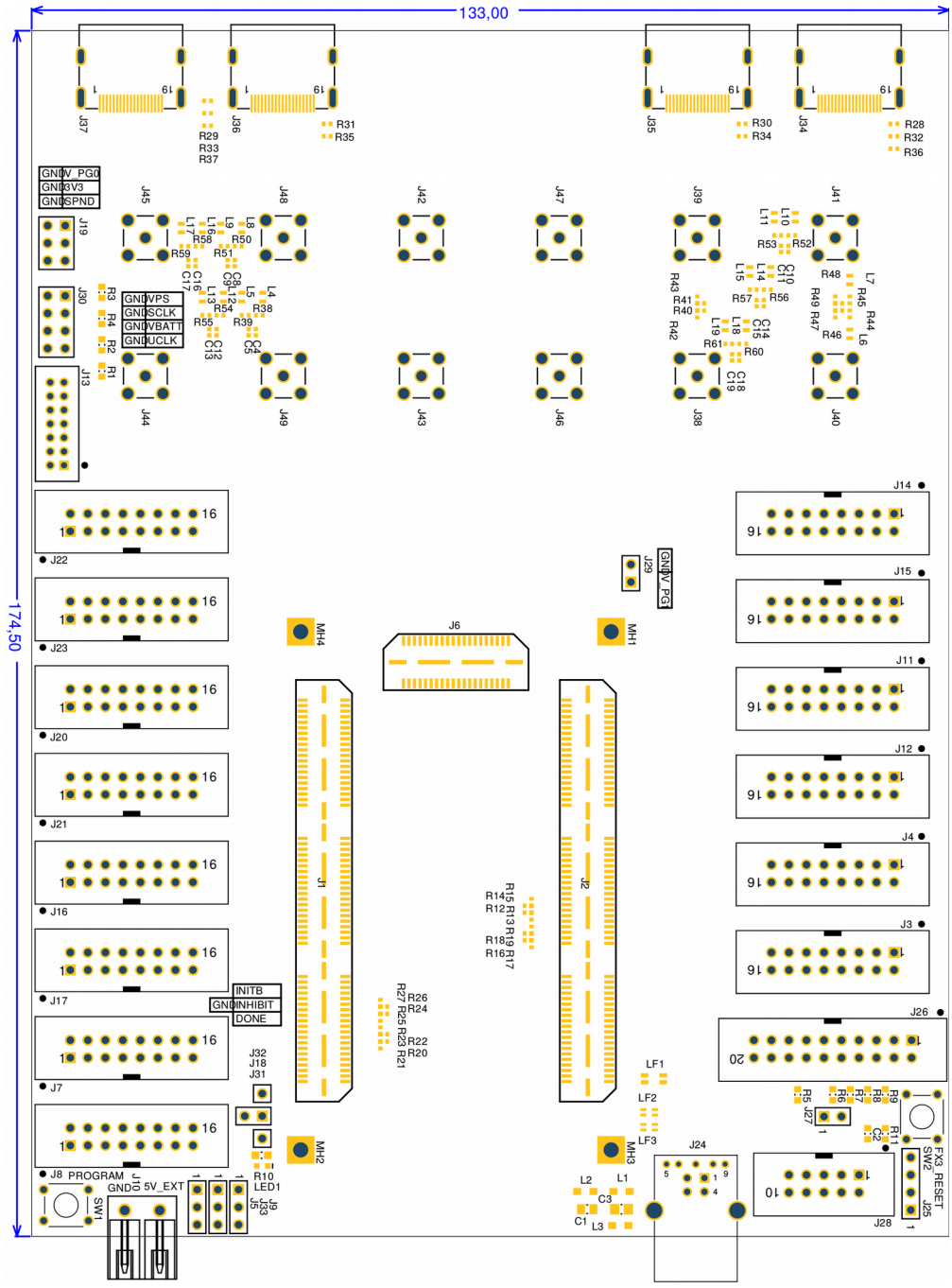


Figure 6: EFM-03 breakout board connectors

Power supply options

The EFM-03 breakout board supports all power supply options of the EFM-03 modules. Jumpers J5, J9 and J33 are used to select the appropriate power scheme. J10 serves as input for an optional external 5.0 V power supply.

J5 - FPGA power on sequence select		
Jumper Position	**Power on sequence**	**Comment**
1-2	USB- controlled	
2-3	Instant on	Requires external power supply

J9 - Power source select EFM-03 or Breakout Board		
Jumper Position	**Power scheme**	**Power supply**
1-2	Bus-powered	USB 3.0 Connector on EFM-03
2-3	Self- or Bus-powered	Selection with J33

J33 - Power source select on Breakout Board		
Jumper Position	**Power scheme**	**Power supply**
1-2	Bus-powered	USB 3.0 Connector J24 on Breakout Board
2-3	Self-powered	External 5.0 V at J10

J10 - External power supply input		
Pin	**Signal**	**Comment**
1	GND	Negative terminal for external power supply
2	5V_EXT	Positive terminal for external 5.0 V power supply

External power supply input requirements				
	Min.	**Typ.**	**Max.**	**Units**
Power supply input range	4.5	5	5.5	V
Minimum current requirement[38]	850			mA

38 FPGA configured with efm03_wrapper design, USB 3.0 transmission to onboard 2 Gbyte DDR3L memory at maximum speed.

JTAG and push-buttons

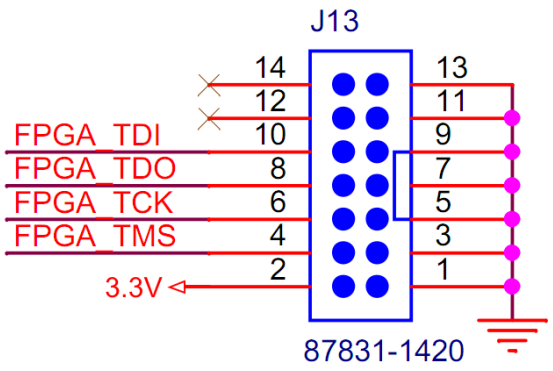


Figure 7: J13 - FPGA JTAG

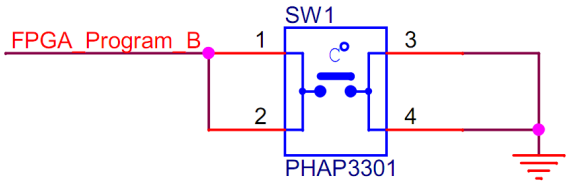


Figure 8: SW1 - FPGA Program_B

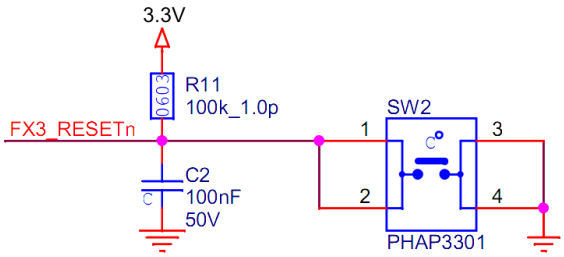


Figure 9: SW2 - EZ-FX3 Reset

With the 14-pin 2 mm connector J13 the EFM-03 breakout board supports standard Xilinx™ JTAG download cables. With the help of the free Xilinx™ Vivado WebPack the FPGA and the attached SPI flash can be programmed. Once the SPI flash is programmed with a valid bitstream, reprogramming of the FPGA can be initiated by pressing the push-button SW1.

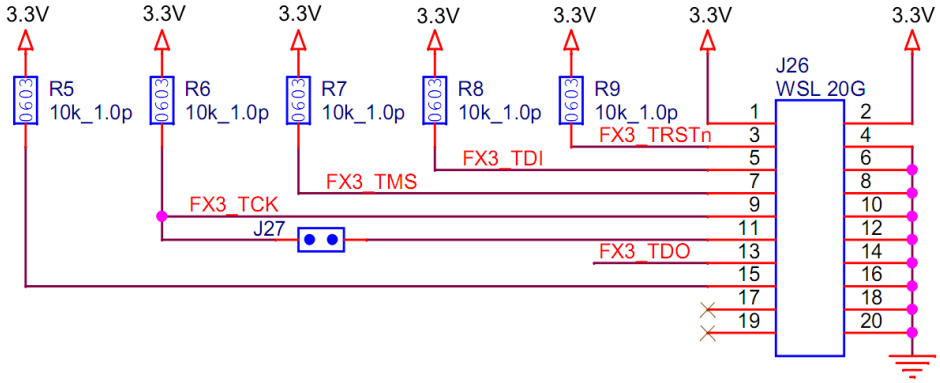


Figure 10: EZ-USB FX3 JTAG

Additionally, the EZ-USB FX3 JTAG interface is routed to J26, a standard 2.54 mm 20-pin shrouded header. This allows direct connection of the JTAG/SWD Emulator with USB interface from Segger, which is recommended by Cypress™. For more details please refer to the FX3 Programmers Manual within EZ-USB FX3 Software Development Kit. To hard reset EZ-USB FX3 press the push-button SW2.

EZ-USB FX3 GPIO and I²C

The general purpose inputs/outputs GPIO55 and GPIO56 of the Cypress™ EZ-USB FX3 controller are available at the shrouded header J28. The optionally usable watchdog timer inside FX3 may be optionally supplied by an external 32 kHz clock source. The associated CLKIN32 input is accessible at pin three of connector J28. EFM-03 uses the I²C EEPROM AT24CM01-XHM from Atmel to store VID/PID data. To increase available storage for larger firmware files EZ-USB FX3 supports multiple devices of the same size and type sharing the I²C bus. On more information about boot options using the I²C interface please consult AN76405 from Cypress™.

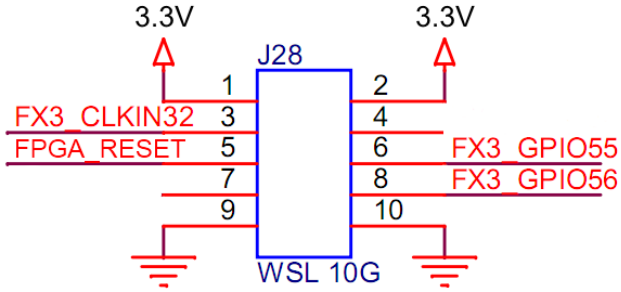


Figure 11: FX3 GPIO signals

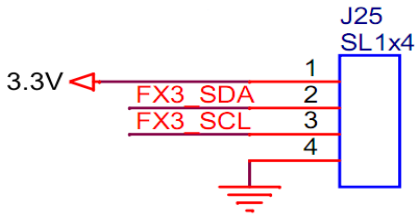


Figure 12: EZ-USB FX3 I²C connector

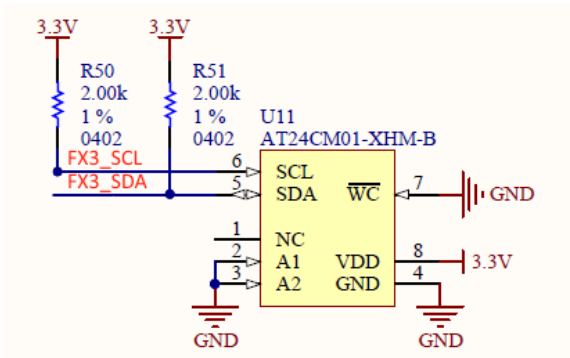


Figure 13: EZ-USB FX3 I²C EEPROM on EFM-03 module

FPGA input-output-signals

Except 'IO_L24P_T3_15' (FPGA ball J25) located at pin 12 of the EFM-03 expansion connector J1, which is connected to the green led LED1 onboard the EFM-03 breakout board, all other FPGA digital IO signals are routed to standard 2.54 mm through-hole shrouded headers for easy access. To prevent FPGA bootup from flash you can assert Flash_Inhibit_n by applying jumper J18, while test pins are available for the FPGA bank supplies VCCO_PG0[39], VCCO_PG1[39], VCCO_3V3[40] and FPGA status signals Init_B and Done.

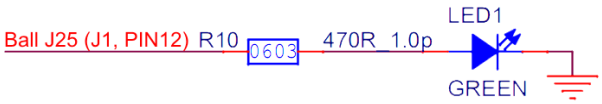


Figure 14: Green user led on EFM-03 breakout board.

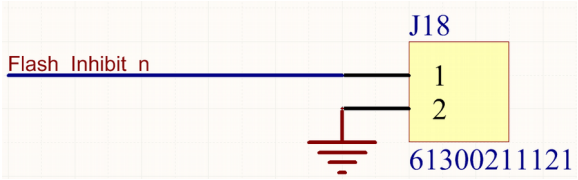


Figure 15: Jumper for Flash_Inhibit_n

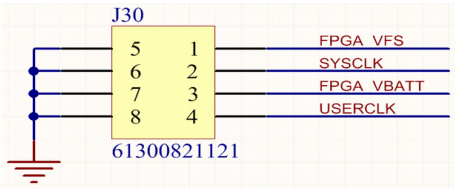


Figure 16: J30 with signals FPGA_VFS, SYSCLK, FPGA_VCCBAT, USERCLK

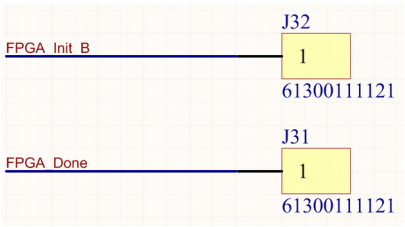


Figure 17: FPGA: Init_B and Done signals

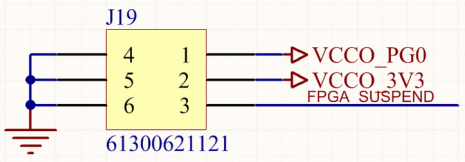


Figure 18: J19

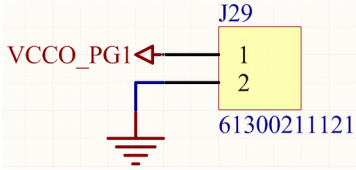


Figure 19: VCCO_PG1

39 To support signal levels other than the default 3.3 V LVTTL, EFM-03 pin groups PG0 and PG1 can optionally be supplied by an external voltage of the required level. **BE SURE to remove** resistors R104 and/or R105 on EFM-03 before applying any voltages to VCCO_PG0 or VCCO_PG1. For details about signal levels supported by Xilinx™ 7 Series FPGAs, please refer to guide ug471.

40 J19,Pin2 for VCCO_3V3 is for the purpose of measuring the supply voltage of pin group PG2 only. **DO NOT connect** external power supplies.

J14 - odd					J14 - even				
Pin	**FPGA Ball**	**Pin Group[41]**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group[41]**	**EXP**	**Description**
1	C23	PG1, IO16N	J2, 53	L19N_T3_VREF_16	**2**	C22	PG1, IO16P	J2, 55	L19P_T3_16
3	AA2	PG1, IO29N	J2, 108	L12N_T1_MRCC_33	**4**	AA3	PG1, IO29P	J2, 106	L12P_T1_MRCC_33
5	H14	PG1, IO0P	J2, 112	L1P_T0_16	**6**	H15	PG1, IO0N	J2, 110	L1N_T0_16
7	B19	PG1, IO9P	J2, 116	L10P_T1_16	**8**	A19	PG1, IO9N	J2, 114	L10N_T2_16
9	Y3	PG1, IO36N	J2, 117	L5P_T0_33	**10**	W3	PG1, IO36P	J2, 119	L5N_T0_33
11	V3	PG1, IO39P	J2, 113	L3P_T0_DQS_33	**12**	V2	PG1, IO39N	J2, 115	L3N_T0_DQS_33
13	Y7	PG1, IO33P	J2, 109	L19P_T3_33	**14**	AA7	PG1, IO33N	J2, 111	L19N_T3_VREF_33
15				**GND**	**16**				**GND**

J15 - odd					J15 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	G16	PG1, IO5N	J2, 73	IO_L6N_T0_VREF_16	**2**	H16	PG1, IO5P	J2, 75	IO_L6P_T0_16
3	F18	PG1, IO2P	J2, 84	IO_L3P_T0_DQS_16	**4**	F19	PG1,IO2N	J2, 82	IO_L3N_T0_DQS_16
5	F17	PG1, IO1N	J2, 88	IO_L2N_T0_16	**6**	G17	PG1, IO1P	J2, 86	IO_L2P_T0_16
7	B17	PG1, IO6N	J2, 92	IO_L7N_T1_16	**8**	C17	PG1, IO6P	J2, 90	IO_L7P_T1_16
9	E16	PG1, IO7P	J2, 96	IO_L8P_T1_16	**10**	D16	PG1, IO7N	J2, 94	IO_L8N_T1_16
11	B20	PG1, IO11P	J2, 100	IO_L15P_T2_DQS_16	**12**	A20	PG1, IO11N	J2, 98	IO_L15N_T2_DQS_16
13	G15	PG1, IO3P	J2, 104	IO_L4P_T0_16	**14**	F15	PG1, IO3N	J2, 102	IO_L4N_T0_16
15				**GND**	**16**				**GND**

J11 - odd					J11 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	D21	PG1, IO15N	J2, 65	IO_L18N_T2_16	**2**	E21	PG1, IO15P	J2, 67	IO_L18P_T2_16
3	C24	PG1, IO22P	J2, 72	IO_L23P_T3_16	**4**	B24	PG1, IO22N	J2, 70	IO_L23N_T3_16
5	A18	PG1, IO8N	J2, 69	IO_L9N_T1_DQS_16	**6**	A17	PG1, IO8P	J2, 71	IO_L9P_T1_DQS_16
7	C18	PG1, IO17N	J2, 77	IO_L12N_T1_MRCC_16	**8**	D18	PG1, IO17P	J2, 79	IO_L12P_T1_MRCC_16
9			**J2, 63**	**1.2 Volt**	**10**			**J2, 61**	**1.2 Volt**
11	D19	PG1, I18P	J2, 80	IO_L13P_T2_MRCC_16	**12**	C19	PG1, IO18N	J2, 78	IO_L13N_T2_MRCC_16
13	G19	PG1, IO4P	J2, 76	IO_L5P_T0_16	**14**	F20	PG1, IO4N	J2, 74	IO_L5N_T0_16
15				**GND**	**16**				**GND**

41 FPGA IO within one specific pin group are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.

J12 - odd					J12 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	A25	PG1, IO19N	J2, 48	IO_L20N_T3_16	**2**	B25	PG1, IO19P	J2, 46	IO_L20P_T3_16
3	A23	PG1, IO20P	J2, 52	IO_L21P_T3_DQS_16	**4**	A24	PG1, IO20N	J2, 50	IO_L21N_T3_DQS_16
5	A22	PG1, IO13N	J2, 56	IO_L17N_T2_16	**6**	B22	PG1, IO13P	J2, 54	IO_L17P_T2_16
7	B21	PG1, IO12N	J2, 60	IO_L16N_T2_16	**8**	C21	PG1, IO12P	J2, 58	IO_L16P_T2_16
9	G20	PG2, IO16P	J2, 64	IO_L11P_T1_SRCC_15	**10**	G21	PG2, IO16N	J2, 62	IO_L11N_T1_SRCC_15
11	E20	PG1, IO10P	J2, 68	IO_L14P_T1_SRCC_16	**12**	D20	PG1, IO10N	J2, 66	IO_L14N_T1_SRCC_16
13	D23	PG1, IO23P	J2, 51	IO_L24P_T3_16	**14**	D24	PG1, IO23N	J2, 49	IO_L24N_T3_16
15				**GND**	**16**				**GND**

J4 - odd					J4 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	K22	PG2, IO4P	J2, 35	IO_L18P_T2_15	**2**	K23	PG2, IO4N	J2, 33	IO_L18N_T2_15
3	F22	PG2, IO19N	J2, 59	IO_L15N_T2_DQS_15	**4**	G22	PG2, IO19P	J2, 57	IO_L15P_T2_DQS_15
5	F24	PG2, IO5N	J2, 47	IO_L19N_T3_15	**6**	G24	PG2, IO5P	J2, 45	IO_L19P_T3_15
7	J23	PG2, IO18P	J2, 37	IO_L14P_T2_SRCC_15	**8**	H23	PG2, IO18N	J2, 39	IO_L14N_T2_SRCC_15
9	M15	PG2, IO1P	J1, 16	IO_L5P_T0_AD9P_15	**10**	L15	PG2, IO1N	J2, 14	IO_L5N_T0_AD9N_15
11	L17	PG2, IO13P	J1, 20	IO_L8P_T1_AD10P_15	**12**	L18	PG2, IO13N	J2, 18	IO_L8N_T1_AD10N_15
13	J21	PG2, IO12N	J2, 43	IO_L12N_T1_MRCC_15	**14**	K21	PG2, IO12P	J2, 41	IO_L12P_T1_MRCC_15
15				**GND**	**16**				**GND**

J3 - odd					J3 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	J20	PG2, IO14N	J2, 28	IO_L09N_T1_DQS_ AD3N_15	**2**	K20	PG2, IO14P	J2, 26	IO_L09P_T1_DQS_ AD3P_15
3	E23	PG2, IO3N	J2, 32	IO_L17N_T2_15	**4**	F23	PG2, IO3P	J2, 30	IO_L17P_T2_15
5	H21	PG2, IO17P	J2, 36	IO_L13P_T2_MRCC_15	**6**	H22	PG2, IO17N	J2, 34	IO_L13N_T2_MRCC_15
7	H19	PG2, IO11N	J2, 40	IO_L7N_T1_AD2N_15	**8**	J19	PG2, IO11P	J2, 38	IO_L7P_T1_AD2P_15
9	D26	PG2, IO7N	J2, 27	IO_L21N_T3_DQS_15	**10**	E26	PG2, IO7P	J2, 25	IO_L21P_T3_DQS_15
11	D25	PG2, IO6N	J2, 31	IO_L20N_T3_15	**12**	E25	PG2, IO6P	J2, 29	IO_L20P_T3_15
13	B26	PG1, IO21N	J2, 44	IO_L22N_T3_16	**14**	C26	PG1, IO21P	J2, 42	IO_L22P_T3_16
15				**GND**	**16**				**GND**

J22 - odd					J22 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	AC2	PG1, IO30N	J1, 108	IO_L11N_T1_SRCC_33	**2**	AB2	PG1, IO30P	J1, 106	IO_L11P_T1_SRCC_33
3	AD3	PG1, IO27N	J1, 100	IO_L14N_T2_SRCC_33	**4**	AC6	PG1, IO34N	J1, 97	IO_L24N_T3_33
5	V6	PG1, IO37P	J2, 105	IO_L4P_T0_33	**6**	W6	PG1, IO37N	J2, 107	IO_L4N_T0_33
7	AA4	PG1, IO28P	J2, 101	IO_L13P_T2_MRCC_33	**8**	AB4	PG1, IO28N	J2, 103	IO_L13N_T2_MRCC_33
9				Not connected	**10**	AC3	PG1, IO27P	J1, 98	IO_L14P_T2_SRCC_33
11	AA8	PG1, IO40N	J2, 93	IO_L23N_T3_33	**12**	Y8	PG1, IO40P	J2, 95	IO_L23P_T3_33
13	E17	PG1, IO14P	J2, 97	IO_L11P_T1_SRCC_16	**14**	E18	PG1, IO14N	J2, 99	IO_L11N_T1_SRCC_16
15				**GND**	**16**				**GND**

J23 - odd					J23 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	AD1	PG1, IO32P	J1, 112	IO_L9P_T1_DQS_33	**2**	AE1	PG1, IO32N	J1, 110	IO_L9N_T1_DQS_33
3	AC4	PG1, IO38P	J1, 95	IO_L18P_T2_33	**4**	AD4	PG1, IO38N	J1, 93	IO_L18N_T2_33
5	U16	PG0, IO20N	J1, 101	IO_L22N_T3_13	**6**	U15	PG0, IO20P	J1, 103	IO_L22P_T3_13
7	AF5	PG1, IO24P	J1, 105	IO_L17P_T2_33	**8**	AF4	PG1, IO24N	J1, 107	IO_L17N_T2_33
9				Not connected	**10**	AB6	PG1, IO34P	J1, 99	IO_L24P_T3_33
11	AE2	PG1, IO31P	J1, 118	IO_L10P_T1_33	**12**	AF2	PG1, IO31N	J1, 120	IO_L10N_T1_33
13	U7	PG1, IO35P	J2, 89	IO_L6P_T0_33	**14**	V7	PG1, IO35N	J2, 91	IO_L6N_T0_VREF_33
15				**GND**	**16**				**GND**

J20 - odd					J20 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	J18	PG2, IO15P	J1, 66	IO_L10P_T1_ AD11P_15	**2**	T17	PG0, IO19P	J1, 80	IO_L21P_T3_DQS_13
3	AE5	PG1, IO26N	J1, 85	IO_L15N_T2_DQS_33	**4**	AD5	PG1, IO26P	J1, 87	IO_L15P_T2_DQS_33
5	V17	PG0, IO22N	J1, 89	IO_L24N_T3_13	**6**	V16	PG0, IO22P	J1, 91	IO_L24P_T3_13
7	V14	PG0, IO21N	J1 86	IO_L23N_T3_13	**8**	U14	PG0, IO21P	J1, 88	IO_L23P_T3_13
9	T15	PG0, IO18N	J1, 90	IO_L20N_T3_13	**10**	T14	PG0, IO18P	J1, 92	IO_L20P_T3_13
11	U21	PG0, IO12P	J1, 94	IO_L13P_T2_ MRCC_13	**12**	V21	PG0, IO12N	J1, 96	IO_L13N_T2_ MRCC_13
13	AF3	PG1, 25N	J1, 102	IO_L16N_T2_33	**14**	AE3	PG1, IO25P	J1, 104	IO_L16P_T2_33
15				**GND**	**16**				**GND**

J21 - odd					J21 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	H18	PG2, IO15N	J1, 68	IO_L10N_T1_AD11N_15	**2**	T18	PG0, IO19N	J1, 78	IO_L21N_T3_DQS_13
3	T19	PG0, IO15P	J1, 73	IO_L17P_T2_13	**4**	U19	PG0, IO15N	J1, 75	IO_L17N_T2_13
5	W19	PG0, IO16N	J1, 77	IO_L18N_T2_13	**6**	V19	PG0, IO16P	J1, 79	IO_L18P_T2_13
7	AC18	PG0, IO25P	J1, 76	IO_L15P_T2_DQS_12	**8**	AD18	PG0, IO25N	J1, 74	IO_L15N_T2_DQS_12
9	AC19	PG0, IO26P	J1, 72	IO_L14P_T2_SRCC_12	**10**	AD19	PG0, IO26N	J1, 70	IO_L14N_T2_SRCC_12
11	AB26	PG0, IO3P	J1, 52	IO_L3P_T0_DQS_13	**12**	AC26	PG0, IO3N	J1, 50	IO_L3N_T0_DQS_13
13	W18	PG0, IO17N	J1, 81	IO_L19N_T3_VREF_13	**14**	V18	PG0, IO17P	J1, 83	IO_L19P_T3_13
15				**GND**	**16**				**GND**

J16 - odd					J16 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	T20	PG0, IO13P	J1, 69	IO_L15P_T2_DQS_13	**2**	U20	PG0, IO13N	J1, 71	IO_L15N_T2_DQS_13
3	AB24	PG0, IO10P	J1, 54	IO_L9P_T1_DQS_13	**4**	AC24	PG0, IO10N	J1, 56	IO_L9N_T1_DQS_13
5	AB21	PG0, IO28P	J1, 58	IO_L11P_T1_SRCC_12	**6**	AC21	PG0, IO28N	J1, 60	IO_L11N_T1_SRCC_12
7	Y20	PG0, IO14N	J1, 62	IO_L16N_T2_13	**8**	W20	PG0, IO14P	J1, 64	IO_L16P_T2_13
9	AB19	PG0, IO33N	J1, 65	IO_L13N_T2_MRCC_12	**10**	AA19	PG0, IO33P	J1, 67	IO_L13P_T2_MRCC_12
11	AE18	PG0, IO24P	J1, 61	IO_L16P_T2_12	**12**	AF18	PG0, IO24N	J1, 63	IO_L16N_T2_12
13	AF20	PG0, IO31N	J1, 57	IO_L8N_T1_12	**14**	AF19	PG0, IO31P	J1, 59	IO_L8P_T1_12
15				**GND**	**16**				**GND**

J17 - odd					J17 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	AD20	PG0, IO29P	J1, 53	IO_L10P_T1_12	**2**	AE20	PG0, IO29N	J1, 55	IO_L10N_T1_12
3	AE22	PG0, IO30P	J1, 49	IO_L9P_T1_DQS_12	**4**	AF22	PG0, IO30N	J1, 51	IO_L9N_T1_DQS_12
5	AD21	PG0, IO32P	J1, 45	IO_L7P_T1_12	**6**	AE21	PG0, IO32N	J1, 47	IO_L7N_T1_12
7	Y21	PG0, IO23N	J1, 40	IO_L14N_T2_MRCC_13	**8**	W21	PG0, IO23P	J1, 38	IO_L14P_T2_MRCC_13
9	U25	PG0, IO0P	J1, 48	IO_L1P_T0_13	**10**	U26	PG0, IO0N	J1, 46	IO_L1N_T0_13
11	W26	PG0, IO2N	J1, 44	IO_L2N_T0_13	**12**	V26	PG0, IO2P	J1, 42	IO_L2P_T0_13
13	AA20	PG0, IO27P	J1, 41	IO_L12P_T1_MRCC_12	**14**	AB20	PG0, IO27N	J1, 43	IO_L12N_T1_MRCC_12
15				**GND**	**16**				**GND**

J7 - odd					J7 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	G25	PG2, IO9P	J1, 3	IO_L23P_T3_15	**2**	F25	PG2, IO9N	J1, 1	IO_L23N_T3_15
3	H26	PG2, IO8P	J1, 7	IO_L22P_T3_15	**4**	G25	PG2, IO8N	J1, 5	IO_L22N_T3_15
5	L14	PG2, IO0N	J1, 26	IO_L4N_T0_15	**6**	M14	PG2, IO2P	J1, 28	IO_L4P_T0_15
7	V23	PG0, IO11P	J1, 30	IO_L10P_T1_13	**8**	W23	PG0, IO11N	J1, 32	IO_L10N_T1_13
9	Y25	PG0, IO6P	J1, 34	IO_L5P_T0_13	**10**	AA25	PG0, IO6N	J1, 36	IO_L5N_T0_13
11	U22	PG0, IO5P	J1, 37	IO_L12P_T1_MRCC_13	**12**	V22	PG0, IO5N	J1, 39	IO_L12N_T1_MRCC_13
13	AB25	PG0, IO8N	J1, 33	IO_L7N_T1_13	**14**	AA24	PG0, IO8P	J1, 35	IO_L7P_T1_13
15				**GND**	**16**				**GND**

J8 - odd					J8 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	H24	PG2, IO2N	J1, 9	IO_L16N_T2_15	**2**	J24	PG2, IO2P	J1, 11	IO_L16P_T2_15
3			**J1, 13**	**1.8 Volt**	**4**			**J1, 15**	**1.8 Volt**
5	M17	PG2, IO10N	J1, 22	IO_L6N_T0_15	**6**	M16	PG2, IO10P	J1, 24	IO_L6P_T0_15
7	AA23	PG0, IO9N	J1, 29	IO_L8N_T1_13	**8**	AA22	PG0, IO9P	J1, 31	IO_L8P_T1_13
9	V24	PG0, IO7P	J1, 25	IO_L6P_T0_13	**10**	W24	PG0, IO7N	J1, 27	IO_L6N_T0_VREF_13
11	Y23	PG0, IO1N	J1, 21	IO_L11N_T1_SRCC_13	**12**	Y22	PG0, IO1P	J1, 23	IO_L11P_T1_SRCC_13
13	Y26	PG0, IO4N	J1, 17	IO_L4N_T0_13	**14**	W25	PG0, IO4P	J1, 19	IO_L4P_T0_13
15				**GND**	**16**				**GND**

FPGA GTP data signals

All GTP data-pins of quad transceivers MGT216 and MGT213 are routed to HDMI connectors J34, J35, J36 and J37. All four diffpairs of a direction-group are routed to the same HDMI connector. Optionally the signals MGTPRX1_N, MGTPRX1_P, MGTPTX2_N and MGTPTX2_P of MGT216 can be wired to SMA connectors, which aren't fitted by default. All RX signals can be fitted with a passive network to adapt to HDMI voltage levels (see XAPP1077, Passive Network 1).

J34 – MGT216 RX			
Pin	**Signal**	**EXP**	**FPGA Ball**
1	MGT216RX3_P	J6-14	D12
2	**GND**	**-**	**-**
3	MGT216RX3_N	J6-16	C12
4	MGT216RX0_P	J6-10	B11
5	**GND**	**-**	**-**
6	MGT216RX0_N	J6-12	A11
7	MGT216RX2_P	J6-6	B13
8	**GND**	**-**	**-**
9	MGT216RX2_N	J6-8	A13
10	MGT216RX1_P	J6-2	D14
11	**GND**	**-**	**-**
12	MGT216RX1_N	J6-4	C14
13	NC	-	-
14	NC	-	-
15	MGT216RX_SCL	J2-47	F24
16	MGT216RX_SDA	J2-45	G24
17	**GND**	**-**	**-**
18	NET_R28_1	-	-
19	NET_R28_2	-	-

J35 – MGT216 TX			
Pin	**Signal**	**EXP**	**FPGA Ball**
1	MGT216TX1_P	J6-15	D8
2	**GND**	**-**	**-**
3	MGT216TX1_N	J6-13	C8
4	MGT216TX0_P	J6-11	B7
5	**GND**	**-**	**-**
6	MGT216TX0_N	J6-9	A7
7	MGT216TX3_P	J6-7	D10
8	**GND**	**-**	**-**
9	MGT216TX3_N	J6-5	C10
10	MGT216TX2_P	J6-3	B9
11	**GND**	**-**	**-**
12	MGT216TX2_N	J6-1	A9
13	NC	-	-
14	NC	-	-
15	MGT216TX_SCL	J2-43	J21
16	MGT216TX_SDA	J2-41	K21
17	**GND**	**-**	**-**
18	NC	-	-
19	**GND**	**-**	**-**

J37 – MGT213 RX			
Pin	**Signal**	**EXP**	**FPGA Ball**
1	MGT213RX2_P	J6-40	AC14
2	**GND**	**-**	**-**
3	MGT213RX2_N	J6-38	AD14
4	MGT213RX0_P	J6-36	AC12
5	**GND**	**-**	**-**
6	MGT213RX0_N	J6-34	AD12
7	MGT213RX1_P	J6-32	AE13
8	**GND**	**-**	**-**
9	MGT213RX1_N	J6-30	AF13
10	MGT213RX3_P	J6-28	AE11
11	**GND**	**-**	**-**
12	MGT213RX3_N	J6-26	AF11
13	NC	-	-
14	NC	-	-
15	MGT213RX_SCL	J1-26	L14
16	MGT213RX_SDA	J1-28	M14
17	**GND**	**-**	**-**
18	NET_R29_1	-	-
19	NET_R29_2	**-**	**-**

J36 – MGT213 TX			
Pin	**Signal**	**EXP**	**FPGA Ball**
1	MGT213TX0_P	J6-37	AC10
2	**GND**	**-**	**-**
3	MGT213TX0_N	J6-39	AD10
4	MGT213TX1_P	J6-33	AE9
5	**GND**	**-**	**-**
6	MGT213TX1_N	J6-35	AF9
7	MGT213TX3_P	J6-29	AE7
8	**GND**	**-**	**-**
9	MGT213TX3_N	J6-31	AF7
10	MGT213TX2_P	J6-25	AC8
11	**GND**	**-**	**-**
12	MGT213TX2_N	J6-27	AD8
13	NC	-	-
14	NC	-	-
15	MGT213TX_SCL	J1-22	M17
16	MGT213TX_SDA	J1-24	M16
17	**GND**	**-**	**-**
18	NC	-	-
19	**GND**	-	-

FPGA GTP reference clock signals

All reference clock input signals are routed to footprints to place SMA connectors. By default these SMA connectors are not fitted.

Reference clock signals from J6			
Pin J6	**Signal**	**FPGA Ball**	**SMA connector**
18	MGT216CLK0_P	F11	J42
20	MGT216CLK0_N	E11	J43
19	MGT216CLK1_P	F13	J47
17	MGT216CLK1_N	E13	J46
21	MGT213CLK0_P	AA13	J44
23	MGT213CLK0_N	AB13	J45
24	MGT213CLK1_P	AA11	J49
22	MGT213CLK1_N	AB11	J48

Selection between HDMI- and SMA-connectors

One RX and one TX diffpair of MGT216 can be routed to SMA connectors. The selection is done with a 0402 sized jumper-resistor.

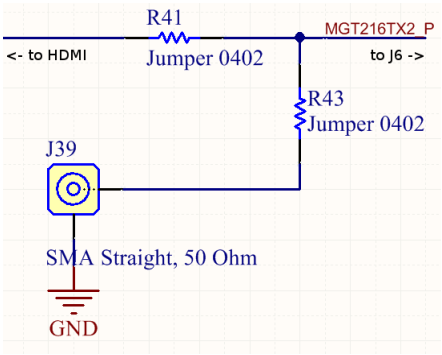


Figure 20: Select HDMI or SMA connector with jumper-resistor

Figure 20 illustrates the wiring from J6 over the resistors to the HDMI- and SMA-connectors for signal MGT216TX2_P. The footprints of R41 and R43 share the pad on the J6-net, so only one position can be fitted at once.

Resistors for connector selection				
Pin J6	**FPGA Ball**	**Signal**	**Select HDMI (default)**	**Select SMA**
4	C14	MGT216RX1_N	R46	R47
2	D14	MGT216RX1_P	R48	R49
1	A9	MGT216TX2_N	R40	R42
3	B9	MGT216TX2_P	R41	R43

SCL and SDA routing to GPIOs

Alike the selection between HDMI and SMA connectors, some GPIO signals can be connected to the SCL and SDA pins of the HDMI connectors or to the shrouded headers. By default the GPIOs are connected to the shrouded headers.

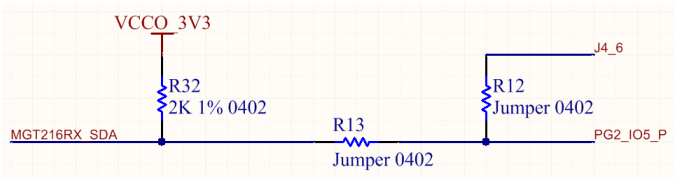


Figure 21: Connect GPIO to shrouded header or SDA/SCL

As an example for all I²C signals, the wiring for MGT216RX_SDA to PG2_IO5_P is shown in Figure 21. Net PG2_IO5_P is wired to the expansion connector J2, pin 45. Net J4_6 is connected to the shrouded header J4, pin 6. The footprints of R12 and R13 share the pad on net PG2_IO5_P. R32 is a pullup resistor to 3.3V. By default only R12 is fitted.

Resistors for GPIO pin wiring to HDMI or shrouded header							
EXP pin	**FPGA Ball**	**GPIO signal**	**HDMI signal**	**Select HDMI**	**Select Header (default)**	**Header pin**	**Optional pullup**
J2-45	G24	PG2_IO5_P	MGT216RX_SDA	R13	R12	J4-6	R32
J2-47	F24	PG2_IO5_N	MGT216RX_SCL	R15	R14	J4-5	R36
J2-41	K21	PG2_IO12_P	MGT216TX_SDA	R17	R16	J4-14	R30
J2-43	J21	PG2_IO12_N	MGT216TX_SCL	R19	R18	J4-13	R34
J1-24	M16	PG2_IO10_P	MGT213TX_SDA	R23	R22	J8-6	R31
J1-22	M17	PG2_IO10_N	MGT213TX_SCL	R21	R20	J8-5	R35
J1-28	M14	PG2_IO0_P	MGT213RX_SDA	R27	R26	J7-6	R33
J1-26	L14	PG2_IO0_N	MGT213RX_SCL	R25	R24	J7-5	R37

EFM-03 on EFM-02/B Breakout Board

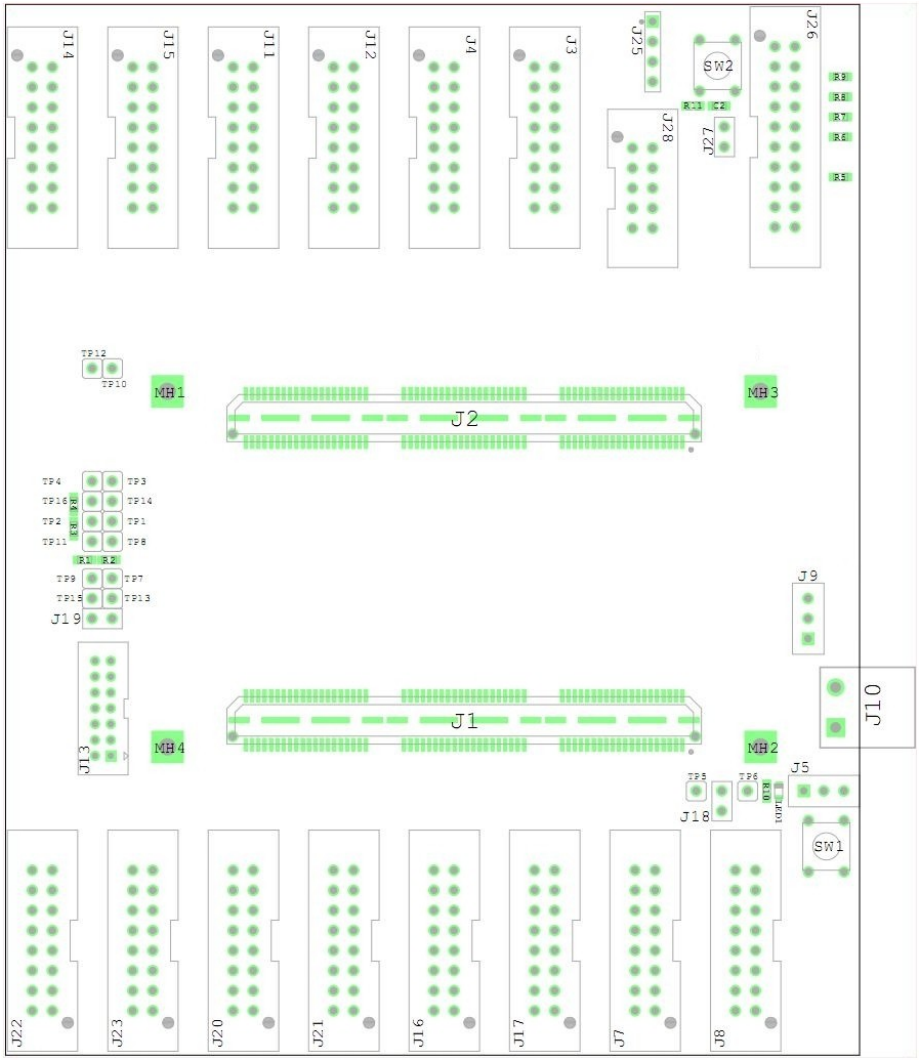


Figure 22: EFM-02/B breakout board connectors

Power supply options

The EFM-02B breakout board supports all power supply options of the EFM-03 modules. Connectors J5 and J9 are used to select the appropriate power scheme. J10 serves as input for an optional external 5.0 V power supply.

J5 - FPGA power on sequence select		
Jumper Position	**Power on sequence**	**Comment**
1-2	USB- controlled	
2-3	Instant on	Requires self-powered mode

J9 - Power source select		
Jumper Position	**Power scheme**	**Power supply**
1-2	Bus-powered	USB 5.0 V VBUS
2-3	Self-powered	External 5.0 V at J10

J10 - External power supply input		
Pin	**Signal**	**Comment**
1	GND	Negative terminal for external power supply
2	5V_EXT	Positive terminal for external 5.0 V power supply

External power supply input requirements				
	Min.	**Typ.**	**Max.**	**Units**
Power supply input range	4.5	5	5.5	V
Minimum current requirement[42]	850			mA

42 FPGA configured with efm03_wrapper design, USB 3.0 transmission to onboard 2 Gbyte DDR3L memory at maximum speed.

JTAG and push-buttons

With the 14-pin 2 mm connector J13 the EFM-02B breakout board supports standard Xilinx™ JTAG download cables. With the help of the free Xilinx™ Vivado WebPack the FPGA and the attached SPI flash can be programmed. Once the SPI flash is programmed with a valid bitstream, reprogramming of the FPGA can be initiated by pressing the push-button SW1.

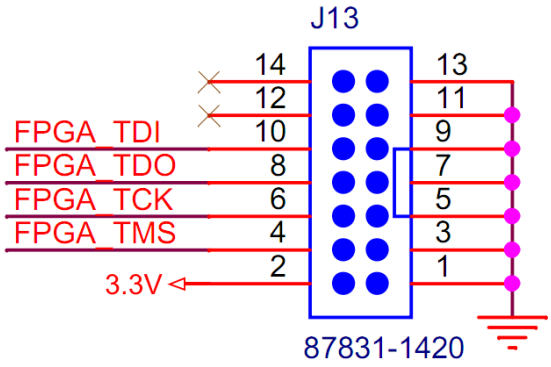


Figure 23: J13 - FPGA JTAG

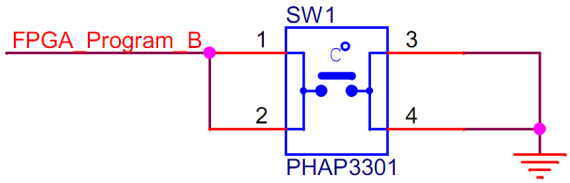


Figure 24: SW1 - FPGA Program_B

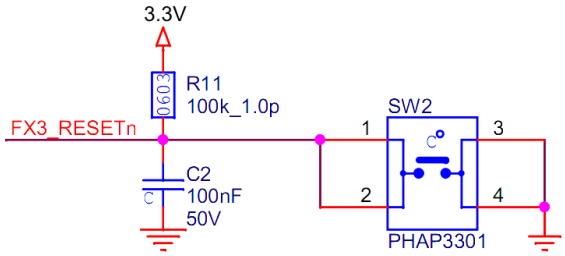


Figure 25: SW2 - EZ-FX3 Reset

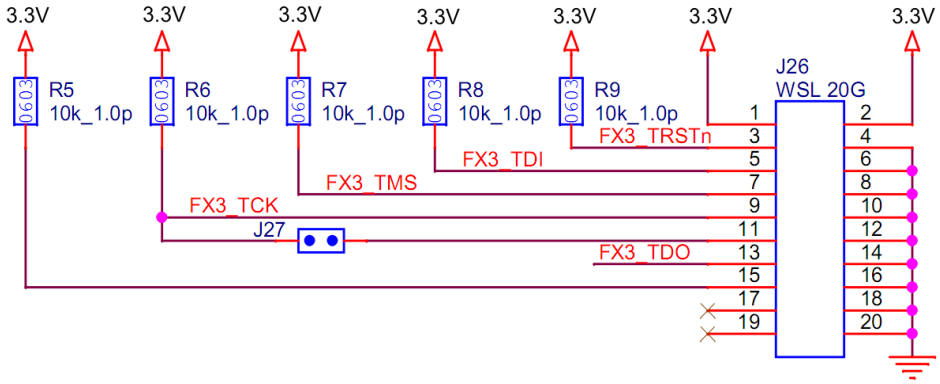


Figure 26: EZ-USB FX3 JTAG

Additionally, the EZ-USB FX3 JTAG interface is routed to J26, a standard 2.54 mm 20-pin shrouded header. This allows direct connection of the JTAG/SWD Emulator with USB interface from Segger, which is recommended by Cypress™. For more details please refer to the FX3 Programmers Manual within EZ-USB FX3 Software Development Kit. To hard reset EZ-USB FX3 press the push-button SW2.

EZ-USB FX3 GPIO and I²C

The general purpose inputs/outputs GPIO55 and GPIO56 of the Cypress™ EZ-USB FX3 controller are available at the shrouded header J28. The optionally usable watchdog timer inside FX3 may be optionally supplied by an external 32 kHz clock source. The associated CLKIN32 input is accessible at pin three of connector J28. EFM-03 uses the I²C EEPROM AT24CM01-XHM from Atmel to store VID/PID data. To increase available storage for larger firmware files EZ-USB FX3 supports multiple devices of the same size and type sharing the I²C bus. On more information about boot options using the I²C interface please consult AN76405 from Cypress™.

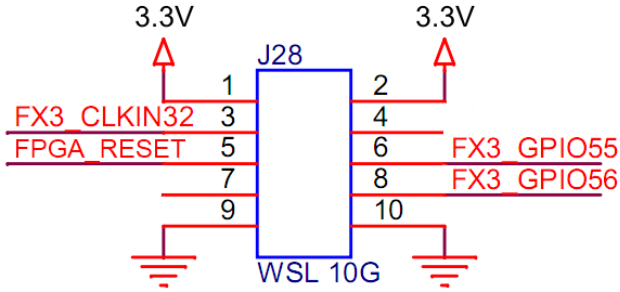


Figure 27: FX3 GPIO signals

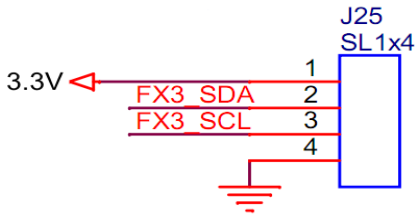


Figure 28: EZ-USB FX3 I²C connector

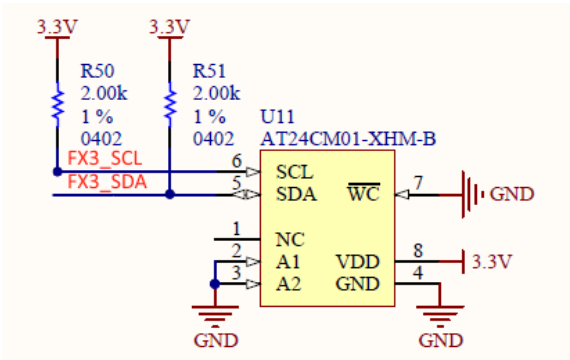


Figure 29: EZ-USB FX3 I²C EEPROM on EFM-03 module

FPGA input-output-signals

Except 'IO_L24P_T3_15' (FPGA ball J25) located at pin 12 of the EFM-03 expansion connector J1, which is connected to the green led LED1 onboard the EFM-02/B breakout board, all other FPGA digital IO signals are routed to standard 2.54 mm through-hole shrouded headers for easy access. To prevent FPGA bootup from flash you can assert Flash_Inhibit_n by applying jumper J18, while test pins are available for the FPGA bank supplies VCCO_PG0[43], VCCO_PG1[43], VCCO_PG2[44] and FPGA status signals Init_B or Done.

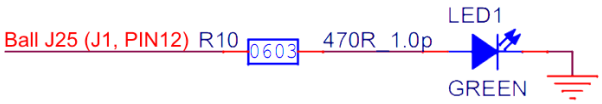


Figure 30: Green user led on EFM-02/B breakout board.

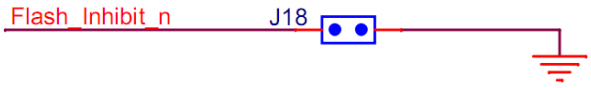


Figure 31: Jumper for Flash_Inhibit_n

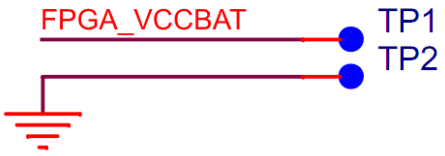


Figure 32: FPGA_VCCBAT

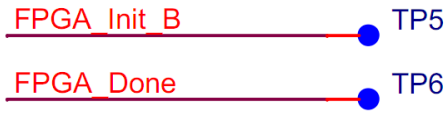


Figure 33: FPGA: Init_B and Done signals

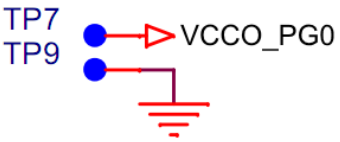


Figure 34: VCCO_PG0

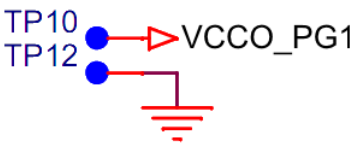


Figure 35: VCCO_PG1

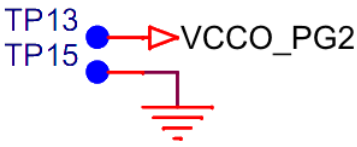


Figure 36: VCCO_PG2

43 To support signal levels other than the default 3.3 V LVTTL, EFM-03 pin groups PG0 and PG1 can optionally be supplied by an external voltage of the required level. **BE SURE to remove** resistors R104 and/or R105 on EFM-03 before applying any voltages to VCCO_PG0 or VCCO_PG1. For details about signal levels supported by Xilinx™ 7 Series FPGAs, please refer to guide ug471.

44 TP13 for VCCO_PG2 is for the purpose of measuring VCCO_PG2 only. **DO NOT connect** external power supplies.

J14 - odd					J14 - even				
Pin	**FPGA Ball**	**Pin Group[45]**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group[45]**	**EXP**	**Description**
1	C23	PG1, IO16N	J2, 53	L19N_T3_VREF_16	**2**	C22	PG1, IO16P	J2, 55	L19P_T3_16
3	AA2	PG1, IO29N	J2, 108	L12N_T1_MRCC_33	**4**	AA3	PG1, IO29P	J2, 106	L12P_T1_MRCC_33
5	H14	PG1, IO0P	J2, 112	L1P_T0_16	**6**	H15	PG1, IO0N	J2, 110	L1N_T0_16
7	B19	PG1, IO9P	J2, 116	L10P_T1_16	**8**	A19	PG1, IO9N	J2, 114	L10N_T2_16
9	Y3	PG1, IO36N	J2, 117	L5P_T0_33	**10**	W3	PG1, IO36P	J2, 119	L5N_T0_33
11	V3	PG1, IO39P	J2, 113	L3P_T0_DQS_33	**12**	V2	PG1, IO39N	J2, 115	L3N_T0_DQS_33
13	Y7	PG1, IO33P	J2, 109	L19P_T3_33	**14**	AA7	PG1, IO33N	J2, 111	L19N_T3_VREF_33
15				**GND**	**16**				**GND**

J15 - odd					J15 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	G16	PG1, IO5N	J2, 73	IO_L6N_T0_VREF_16	**2**	H16	PG1, IO5P	J2, 75	IO_L6P_T0_16
3	F18	PG1, IO2P	J2, 84	IO_L3P_T0_DQS_16	**4**	F19	PG1,IO2N	J2, 82	IO_L3N_T0_DQS_16
5	F17	PG1, IO1N	J2, 88	IO_L2N_T0_16	**6**	G17	PG1, IO1P	J2, 86	IO_L2P_T0_16
7	B17	PG1, IO6N	J2, 92	IO_L7N_T1_16	**8**	C17	PG1, IO6P	J2, 90	IO_L7P_T1_16
9	E16	PG1, IO7P	J2, 96	IO_L8P_T1_16	**10**	D16	PG1, IO7N	J2, 94	IO_L8N_T1_16
11	B20	PG1, IO11P	J2, 100	IO_L15P_T2_DQS_16	**12**	A20	PG1, IO11N	J2, 98	IO_L15N_T2_DQS_16
13	G15	PG1, IO3P	J2, 104	IO_L4P_T0_16	**14**	F15	PG1, IO3N	J2, 102	IO_L4N_T0_16
15				**GND**	**16**				**GND**

J11 - odd					J11 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	D21	PG1, IO15N	J2, 65	IO_L18N_T2_16	**2**	E21	PG1, IO15P	J2, 67	IO_L18P_T2_16
3	C24	PG1, IO22P	J2, 72	IO_L23P_T3_16	**4**	B24	PG1, IO22N	J2, 70	IO_L23N_T3_16
5	A18	PG1, IO8N	J2, 69	IO_L9N_T1_DQS_16	**6**	A17	PG1, IO8P	J2, 71	IO_L9P_T1_DQS_16
7	C18	PG1, IO17N	J2, 77	IO_L12N_T1_MRCC_16	**8**	D18	PG1, IO17P	J2, 79	IO_L12P_T1_MRCC_16
9			**J2, 63**	**1.2 Volt**	**10**			**J2, 61**	**1.2 Volt**
11	D19	PG1, I18P	J2, 80	IO_L13P_T2_MRCC_16	**12**	C19	PG1, IO18N	J2, 78	IO_L13N_T2_MRCC_16
13	G19	PG1, IO4P	J2, 76	IO_L5P_T0_16	**14**	F20	PG1, IO4N	J2, 74	IO_L5N_T0_16
15				**GND**	**16**				**GND**

45 FPGA IO within one specific pin group are powered via the same power supply. PG0 and PG1 power supplies are routed independently and optionally can be powered via the respective expansion pins to support IO signaling levels other than the default 3.3 Volt LVTTL.

J12 - odd					J12 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	A25	PG1, IO19N	J2, 48	IO_L20N_T3_16	**2**	B25	PG1, IO19P	J2, 46	IO_L20P_T3_16
3	A23	PG1, IO20P	J2, 52	IO_L21P_T3_DQS_16	**4**	A24	PG1, IO20N	J2, 50	IO_L21N_T3_DQS_16
5	A22	PG1, IO13N	J2, 56	IO_L17N_T2_16	**6**	B22	PG1, IO13P	J2, 54	IO_L17P_T2_16
7	B21	PG1, IO12N	J2, 60	IO_L16N_T2_16	**8**	C21	PG1, IO12P	J2, 58	IO_L16P_T2_16
9	G20	PG2, IO16P	J2, 64	IO_L11P_T1_SRCC_15	**10**	G21	PG2, IO16N	J2, 62	IO_L11N_T1_SRCC_15
11	E20	PG1, IO10P	J2, 68	IO_L14P_T1_SRCC_16	**12**	D20	PG1, IO10N	J2, 66	IO_L14N_T1_SRCC_16
13	D23	PG1, IO23P	J2, 51	IO_L24P_T3_16	**14**	D24	PG1, IO23N	J2, 49	IO_L24N_T3_16
15				**GND**	**16**				**GND**

J4 - odd					J4 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	K22	PG2, IO4P	J2, 35	IO_L18P_T2_15	**2**	K23	PG2, IO4N	J2, 33	IO_L18N_T2_15
3	F22	PG2, IO19N	J2, 59	IO_L15N_T2_DQS_15	**4**	G22	PG2, IO19P	J2, 57	IO_L15P_T2_DQS_15
5	F24	PG2, IO5N	J2, 47	IO_L19N_T3_15	**6**	G24	PG2, IO5P	J2, 45	IO_L19P_T3_15
7	J23	PG2, IO18P	J2, 37	IO_L14P_T2_SRCC_15	**8**	H23	PG2, IO18N	J2, 39	IO_L14N_T2_SRCC_15
9	M15	PG2, IO1P	J1, 16	IO_L5P_T0_AD9P_15	**10**	L15	PG2, IO1N	J2, 14	IO_L5N_T0_AD9N_15
11	L17	PG2, IO13P	J1, 20	IO_L8P_T1_AD10P_15	**12**	L18	PG2, IO13N	J2, 18	IO_L8N_T1_AD10N_15
13	J21	PG2, IO12N	J2, 43	IO_L12N_T1_MRCC_15	**14**	K21	PG2, IO12P	J2, 41	IO_L12P_T1_MRCC_15
15				**GND**	**16**				**GND**

J3 - odd					J3 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	J20	PG2, IO14N	J2, 28	IO_L09N_T1_DQS_ AD3N_15	**2**	K20	PG2, IO14P	J2, 26	IO_L09P_T1_DQS_ AD3P_15
3	E23	PG2, IO3N	J2, 32	IO_L17N_T2_15	**4**	F23	PG2, IO3P	J2, 30	IO_L17P_T2_15
5	H21	PG2, IO17P	J2, 36	IO_L13P_T2_MRCC_15	**6**	H22	PG2, IO17N	J2, 34	IO_L13N_T2_MRCC_15
7	H19	PG2, IO11N	J2, 40	IO_L7N_T1_AD2N_15	**8**	J19	PG2, IO11P	J2, 38	IO_L7P_T1_AD2P_15
9	D26	PG2, IO7N	J2, 27	IO_L21N_T3_DQS_15	**10**	E26	PG2, IO7P	J2, 25	IO_L21P_T3_DQS_15
11	D25	PG2, IO6N	J2, 31	IO_L20N_T3_15	**12**	E25	PG2, IO6P	J2, 29	IO_L20P_T3_15
13	B26	PG1, IO21N	J2, 44	IO_L22N_T3_16	**14**	C26	PG1, IO21P	J2, 42	IO_L22P_T3_16
15				**GND**	**16**				**GND**

J22 - odd					J22 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	AC2	PG1, IO30N	J1, 108	IO_L11N_T1_SRCC_33	**2**	AB2	PG1, IO30P	J1, 106	IO_L11P_T1_SRCC_33
3	AD3	PG1, IO27N	J1, 100	IO_L14N_T2_SRCC_33	**4**	AC6	PG1, IO34N	J1, 97	IO_L24N_T3_33
5	V6	PG1, IO37P	J2, 105	IO_L4P_T0_33	**6**	W6	PG1, IO37N	J2, 107	IO_L4N_T0_33
7	AA4	PG1, IO28P	J2, 101	IO_L13P_T2_MRCC_33	**8**	AB4	PG1, IO28N	J2, 103	IO_L13N_T2_MRCC_33
9				Not connected	**10**	AC3	PG1, IO27P	J1, 98	IO_L14P_T2_SRCC_33
11	AA8	PG1, IO40N	J2, 93	IO_L23N_T3_33	**12**	Y8	PG1, IO40P	J2, 95	IO_L23P_T3_33
13	E17	PG1, IO14P	J2, 97	IO_L11P_T1_SRCC_16	**14**	E18	PG1, IO14N	J2, 99	IO_L11N_T1_SRCC_16
15				**GND**	**16**				**GND**

J23 - odd					J23 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	AD1	PG1, IO32P	J1, 112	IO_L9P_T1_DQS_33	**2**	AE1	PG1, IO32N	J1, 110	IO_L9N_T1_DQS_33
3	AC4	PG1, IO38P	J1, 95	IO_L18P_T2_33	**4**	AD4	PG1, IO38N	J1, 93	IO_L18N_T2_33
5	U16	PG0, IO20N	J1, 101	IO_L22N_T3_13	**6**	U15	PG0, IO20P	J1, 103	IO_L22P_T3_13
7	AF5	PG1, IO24P	J1, 105	IO_L17P_T2_33	**8**	AF4	PG1, IO24N	J1, 107	IO_L17N_T2_33
9				Not connected	**10**	AB6	PG1, IO34P	J1, 99	IO_L24P_T3_33
11	AE2	PG1, IO31P	J1, 118	IO_L10P_T1_33	**12**	AF2	PG1, IO31N	J1, 120	IO_L10N_T1_33
13	U7	PG1, IO35P	J2, 89	IO_L6P_T0_33	**14**	V7	PG1, IO35N	J2, 91	IO_L6N_T0_VREF_33
15				**GND**	**16**				**GND**

J20 - odd					J20 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	J18	PG2, IO15P	J1, 66	IO_L10P_T1_ AD11P_15	**2**	T17	PG0, IO19P	J1, 80	IO_L21P_T3_DQS_13
3	AE5	PG1, IO26N	J1, 85	IO_L15N_T2_DQS_33	**4**	AD5	PG1, IO26P	J1, 87	IO_L15P_T2_DQS_33
5	V17	PG0, IO22N	J1, 89	IO_L24N_T3_13	**6**	V16	PG0, IO22P	J1, 91	IO_L24P_T3_13
7	V14	PG0, IO21N	J1 86	IO_L23N_T3_13	**8**	U14	PG0, IO21P	J1, 88	IO_L23P_T3_13
9	T15	PG0, IO18N	J1, 90	IO_L20N_T3_13	**10**	T14	PG0, IO18P	J1, 92	IO_L20P_T3_13
11	U21	PG0, IO12P	J1, 94	IO_L13P_T2_ MRCC_13	**12**	V21	PG0, IO12N	J1, 96	IO_L13N_T2_ MRCC_13
13	AF3	PG1, 25N	J1, 102	IO_L16N_T2_33	**14**	AE3	PG1, IO25P	J1, 104	IO_L16P_T2_33
15				**GND**	**16**				**GND**

J21 - odd					J21 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	H18	PG2, IO15N	J1, 68	IO_L10N_T1_AD11N_15	**2**	T18	PG0, IO19N	J1, 78	IO_L21N_T3_DQS_13
3	T19	PG0, IO15P	J1, 73	IO_L17P_T2_13	**4**	U19	PG0, IO15N	J1, 75	IO_L17N_T2_13
5	W19	PG0, IO16N	J1, 77	IO_L18N_T2_13	**6**	V19	PG0, IO16P	J1, 79	IO_L18P_T2_13
7	AC18	PG0, IO25P	J1, 76	IO_L15P_T2_DQS_12	**8**	AD18	PG0, IO25N	J1, 74	IO_L15N_T2_DQS_12
9	AC19	PG0, IO26P	J1, 72	IO_L14P_T2_SRCC_12	**10**	AD19	PG0, IO26N	J1, 70	IO_L14N_T2_SRCC_12
11	AB26	PG0, IO3P	J1, 52	IO_L3P_T0_DQS_13	**12**	AC26	PG0, IO3N	J1, 50	IO_L3N_T0_DQS_13
13	W18	PG0, IO17N	J1, 81	IO_L19N_T3_VREF_13	**14**	V18	PG0, IO17P	J1, 83	IO_L19P_T3_13
15				**GND**	**16**				**GND**

J16 - odd					J16 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	T20	PG0, IO13P	J1, 69	IO_L15P_T2_DQS_13	**2**	U20	PG0, IO13N	J1, 71	IO_L15N_T2_DQS_13
3	AB24	PG0, IO10P	J1, 54	IO_L9P_T1_DQS_13	**4**	AC24	PG0, IO10N	J1, 56	IO_L9N_T1_DQS_13
5	AB21	PG0, IO28P	J1, 58	IO_L11P_T1_SRCC_12	**6**	AC21	PG0, IO28N	J1, 60	IO_L11N_T1_SRCC_12
7	Y20	PG0, IO14N	J1, 62	IO_L16N_T2_13	**8**	W20	PG0, IO14P	J1, 64	IO_L16P_T2_13
9	AB19	PG0, IO33N	J1, 65	IO_L13N_T2_MRCC_12	**10**	AA19	PG0, IO33P	J1, 67	IO_L13P_T2_MRCC_12
11	AE18	PG0, IO24P	J1, 61	IO_L16P_T2_12	**12**	AF18	PG0, IO24N	J1, 63	IO_L16N_T2_12
13	AF20	PG0, IO31N	J1, 57	IO_L8N_T1_12	**14**	AF19	PG0, IO31P	J1, 59	IO_L8P_T1_12
15				**GND**	**16**				**GND**

J17 - odd					J17 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	AD20	PG0, IO29P	J1, 53	IO_L10P_T1_12	**2**	AE20	PG0, IO29N	J1, 55	IO_L10N_T1_12
3	AE22	PG0, IO30P	J1, 49	IO_L9P_T1_DQS_12	**4**	AF22	PG0, IO30N	J1, 51	IO_L9N_T1_DQS_12
5	AD21	PG0, IO32P	J1, 45	IO_L7P_T1_12	**6**	AE21	PG0, IO32N	J1, 47	IO_L7N_T1_12
7	Y21	PG0, IO23N	J1, 40	IO_L14N_T2_MRCC_13	**8**	W21	PG0, IO23P	J1, 38	IO_L14P_T2_MRCC_13
9	U25	PG0, IO0P	J1, 48	IO_L1P_T0_13	**10**	U26	PG0, IO0N	J1, 46	IO_L1N_T0_13
11	W26	PG0, IO2N	J1, 44	IO_L2N_T0_13	**12**	V26	PG0, IO2P	J1, 42	IO_L2P_T0_13
13	AA20	PG0, IO27P	J1, 41	IO_L12P_T1_MRCC_12	**14**	AB20	PG0, IO27N	J1, 43	IO_L12N_T1_MRCC_12
15				**GND**	**16**				**GND**

J7 - odd					J7 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	G25	PG2, IO9P	J1, 3	IO_L23P_T3_15	**2**	F25	PG2, IO9N	J1, 1	IO_L23N_T3_15
3	H26	PG2, IO8P	J1, 7	IO_L22P_T3_15	**4**	G25	PG2, IO8N	J1, 5	IO_L22N_T3_15
5	L14	PG2, IO0N	J1, 26	IO_L4N_T0_15	**6**	M14	PG2, IO2P	J1, 28	IO_L4P_T0_15
7	V23	PG0, IO11P	J1, 30	IO_L10P_T1_13	**8**	W23	PG0, IO11N	J1, 32	IO_L10N_T1_13
9	Y25	PG0, IO6P	J1, 34	IO_L5P_T0_13	**10**	AA25	PG0, IO6N	J1, 36	IO_L5N_T0_13
11	U22	PG0, IO5P	J1, 37	IO_L12P_T1_MRCC_13	**12**	V22	PG0, IO5N	J1, 39	IO_L12N_T1_MRCC_13
13	AB25	PG0, IO8N	J1, 33	IO_L7N_T1_13	**14**	AA24	PG0, IO8P	J1, 35	IO_L7P_T1_13
15				**GND**	**16**				**GND**

J8 - odd					J8 - even				
Pin	**FPGA Ball**	**Pin Group**	**EXP**	**Description**	**Pin**	**FPGA Ball**	**Pin Group**	**EXP**	**Description**
1	H24	PG2, IO2N	J1, 9	IO_L16N_T2_15	**2**	J24	PG2, IO2P	J1, 11	IO_L16P_T2_15
3			**J1, 13**	**1.8 Volt**	**4**			**J1, 15**	**1.8 Volt**
5	M17	PG2, IO10N	J1, 22	IO_L6N_T0_15	**6**	M16	PG2, IO10P	J1, 24	IO_L6P_T0_15
7	AA23	PG0, IO9N	J1, 29	IO_L8N_T1_13	**8**	AA22	PG0, IO9P	J1, 31	IO_L8P_T1_13
9	V24	PG0, IO7P	J1, 25	IO_L6P_T0_13	**10**	W24	PG0, IO7N	J1, 27	IO_L6N_T0_VREF_13
11	Y23	PG0, IO1N	J1, 21	IO_L11N_T1_SRCC_13	**12**	Y22	PG0, IO1P	J1, 23	IO_L11P_T1_SRCC_13
13	Y26	PG0, IO4N	J1, 17	IO_L4N_T0_13	**14**	W25	PG0, IO4P	J1, 19	IO_L4P_T0_13
15				**GND**	**16**				**GND**

Mechanical drawings

EFM-03

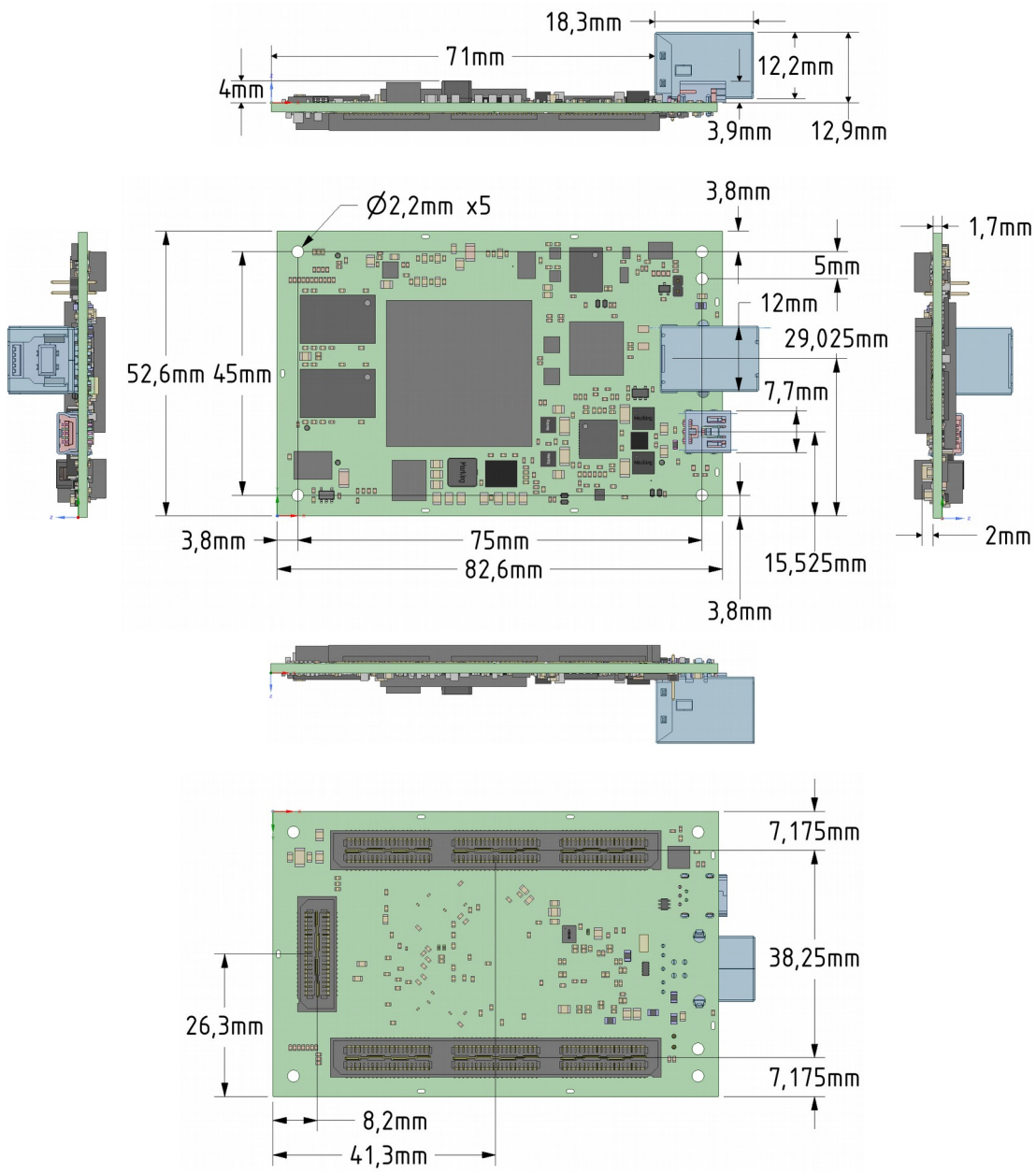


Figure 37: EFM-03 mechanical drawings

The four mounting holes of size M2-fine located in the corners of the PCB are electrically isolated. The fifth mounting hole located next to the USB 3.0 type B connector provides access to the USB shielding.

EFM-03 connector placement

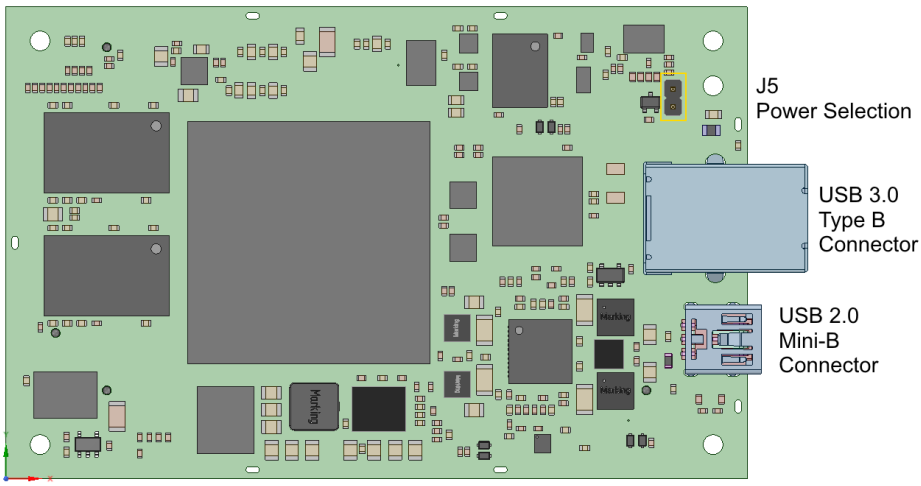


Figure 38: EFM-03 connectors on top (J5, USB 3.0, USB 2.0)

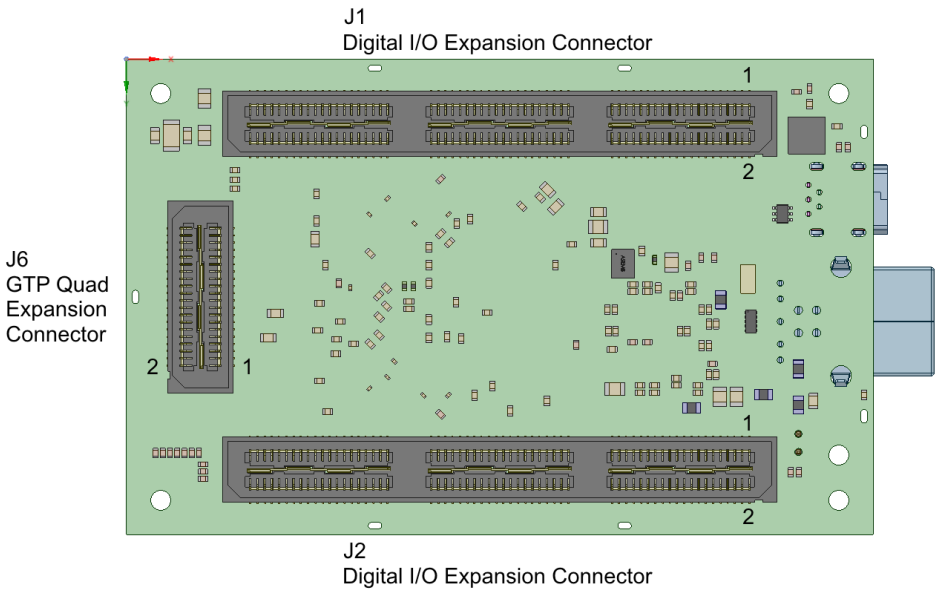


Figure 39: EFM-03 connectors on bottom (J1, J2, J6)

EFM-03 footprint example

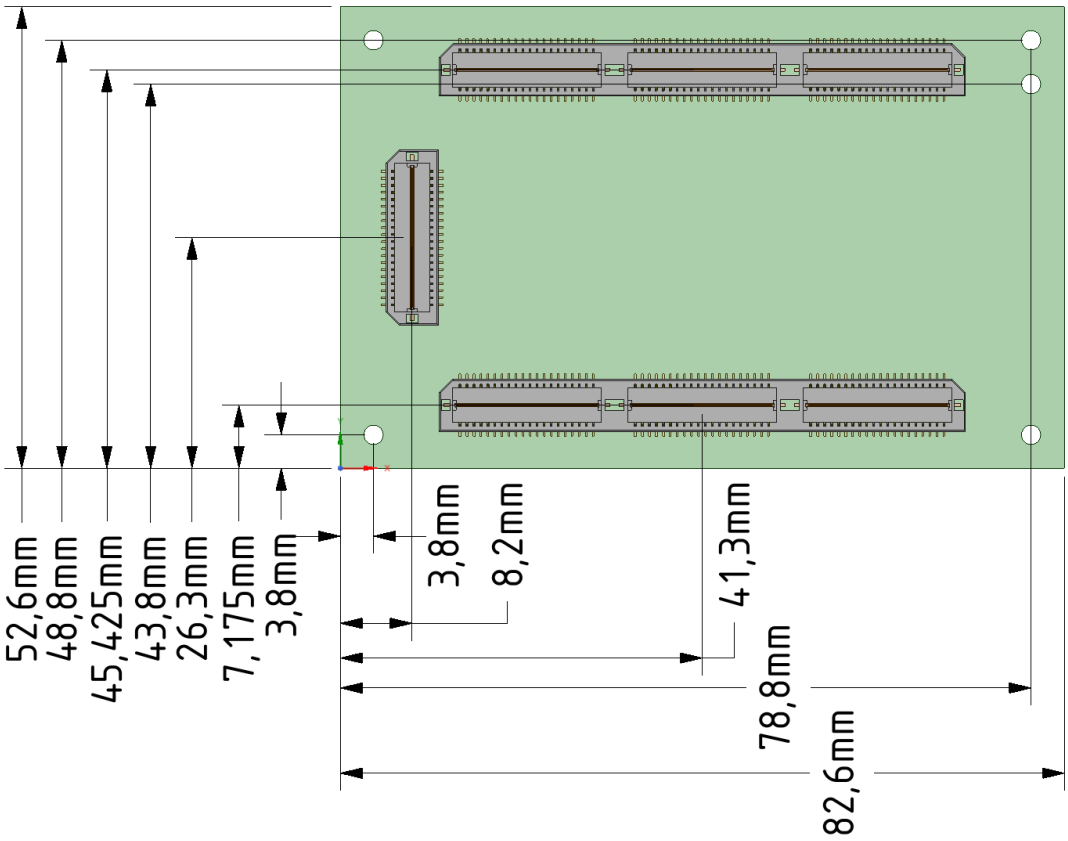


Figure 40: EFM-03 footprint example

Mating connectors

Samtec™ part number J1 & J2	Samtec™ part number J6	Mated height
QTE-060-01-L-D	QTE-020-01-L-D	5.00 mm
QTE-060-02-L-D	QTE-020-02-L-D	8.00 mm
QTE-060-03-L-D	QTE-020-03-L-D	11.00 mm
QTE-060-04-L-D	QTE-020-04-L-D	16.00 mm
QTE-060-05-L-D	QTE-020-05-L-D	19.00 mm
QTE-060-07-L-D	QTE-020-07-L-D	25.00 mm

Ordering information

Order Number	FPGA	VCCO PG0 / PG1	USB 3.0 connector	Comment
C028336	XC7A200T-2FBG676I	Onboard 3.3 Volt	Type B, onboard	Standard

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Revision history

Version	Date	Comment	Author	Approved by
preliminary	April, 2017	Preliminary	mh	mh
v1.0	August, 2017	Removed 'preliminary', added EFM-03 Breakout Board	mh, ds	mh
v1.1	June, 2018	page 24: added footnote for pin J2/16; page 54: added connector names to image captions	ds	mk

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